



# **InsydeH2O Setup Utility Reference Guide For Alder Lake 5.4 Platform**

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Insyde Software Corp.



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## Revision History

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Revision Number	Description	Author	Release Date
<0.1>	Initial release.	Evonne Li	August 30, 2021

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# 1 Introduction

## 1.1 Overview

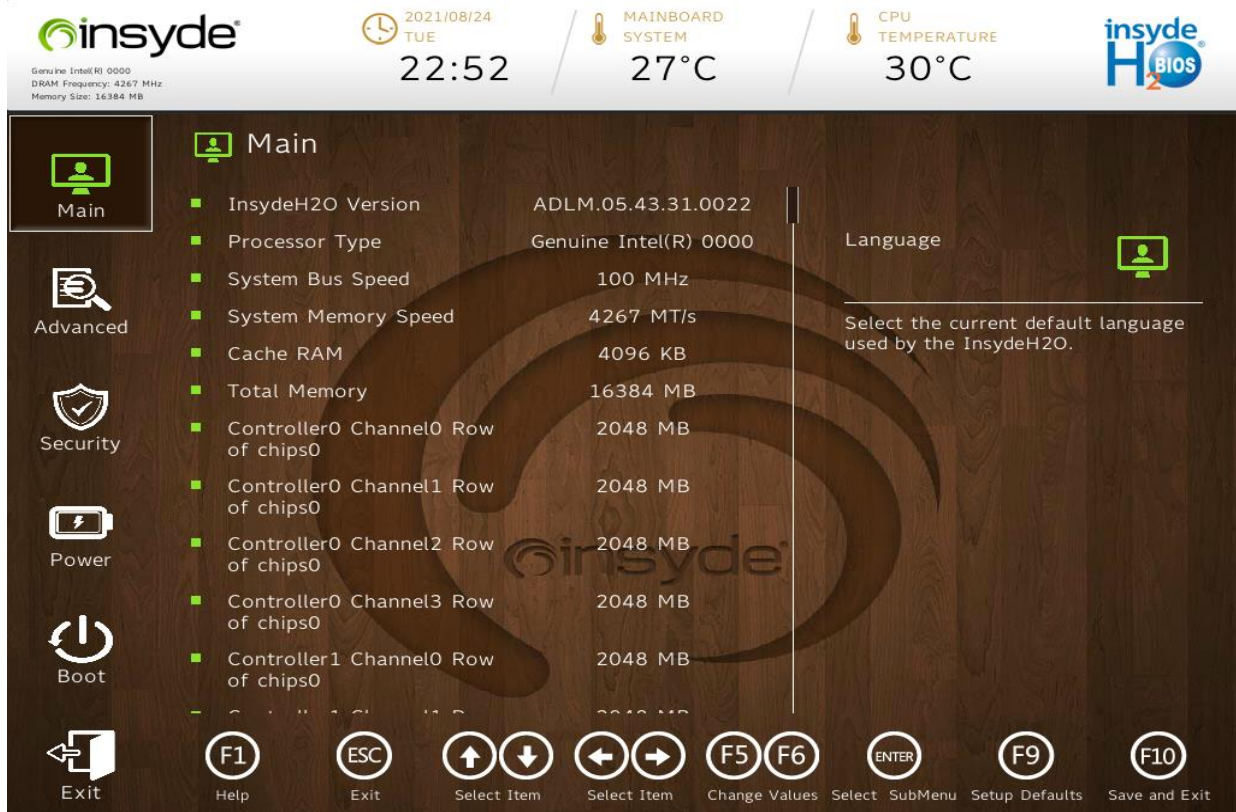
This document explains the InsydeH2O BIOS which displays system configuration settings and allows the changing of these settings to configure the system. The InsydeH2O BIOS Utility consists of a menu-based interface that makes navigating and selecting various BIOS functions a simple process.

The InsydeH2O BIOS Setup Utility can be utilized to view and change BIOS settings for the motherboard. Press <ESC> key on keyboard during the Power-On Self-Test (POST) routine to enter the Front Page and select the SCU item to enter the InsydeH2O BIOS Setup Utility.

Use <←> and <→> keys on the keyboard to navigate to each menu. The <↑> and <↓> arrow keys allow user to navigate to items within each menu. Press <Enter> key to select the item and navigate the item submenu (if available). Use <ESC> key at any time to return to the previous respective submenu or menu. You can also refer to the bottom portion of the InsydeH2O BIOS Setup Utility screen for quick navigation instructions.

Once inside the InsydeH2O Setup Utility, user will see these menu options:

**Figure 1-1. InsydeH2O Setup Utility Items**



**Table 1-1. InsydeH2O Setup Utility Items**

Menu Name	Description
Main	Display system information such as CPU type and speed, system bus speed, system memory speed, total installed memory, current language, and system date & time, etc.
Advanced	Allow configuration of advanced system settings such as boot configuration, ACPI features, and chipset configuration, etc.
Security	Set passwords and security functions.
Power	Configure power management functions.
Boot	Set boot options such as Quick Boot or USB Boot.
Exit	Allow user to save or discard BIOS changes, and load optimal or custom default settings.

If changes made to the BIOS result in system malfunction or undesired system performance, enter the BIOS again and press F9 to load Setup Defaults, and then press F10 to save and exit the BIOS.

## 1.2 BIOS Boot Sequence

User can press <ECS> key when system boot and enter the Front Page select menu (see Figure 1-2), and then do different boot sequences (see Table 1-2).



**Table 1-2. Boot Sequences**

Sequence	Step
Normal boot	<ol style="list-style-type: none"> <li>1. Power on</li> <li>2. Logo Screen</li> <li>3. OS boot</li> </ol>
Boot to BIOS Front Page Screen	<ol style="list-style-type: none"> <li>1. Power on</li> <li>2. Logo Screen</li> <li>3. Press &lt;ESC&gt; key</li> </ol>
Boot to Boot Manager	<ol style="list-style-type: none"> <li>1. Power on</li> <li>2. Logo Screen</li> <li>3. Press &lt;ESC&gt; key</li> <li>4. Select <u>Boot Manager</u> Icon</li> </ol>
Boot to Device Manager	<ol style="list-style-type: none"> <li>1. Power on</li> <li>2. Logo Screen</li> <li>3. Press &lt;ESC&gt; key</li> <li>4. Select <u>Device Manager</u> Icon</li> </ol>
Boot to Boot from File	<ol style="list-style-type: none"> <li>1. Power on</li> <li>2. Logo Screen</li> <li>3. Press &lt;ESC&gt; key</li> <li>4. Select <u>Boot from File</u> Icon</li> </ol>
Boot to Secure Boot	<ol style="list-style-type: none"> <li>1. Power on</li> <li>2. Logo Screen</li> <li>3. Press &lt;ESC&gt; key</li> <li>4. Select <u>Secure Boot Option</u> Icon</li> </ol>
Boot to Setup Utility	<ol style="list-style-type: none"> <li>1. Power on</li> <li>2. Logo Screen</li> <li>3. Press &lt;ESC&gt; key</li> <li>4. Select <u>SCU</u> Icon</li> </ol>
Continue Booting Process	<ol style="list-style-type: none"> <li>1. Power on</li> <li>2. Logo Screen</li> <li>3. Press &lt;ESC&gt; key</li> <li>4. Select <u>Continue</u> Icon</li> </ol>

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## 2 BIOS Setup Utility

The BIOS Setup Utility provides a User Interface to users to set the system configuration.

### 2.1 Main Menu

Main Menu of InsydeH2O BIOS Setup Utility provides a quick overview of basic system information and the ability to change the displayed language and system time, and the copyright description.

**Figure 2-1. Setup Utility Main Menu**



**Table 2-1. Main Menu Setting**

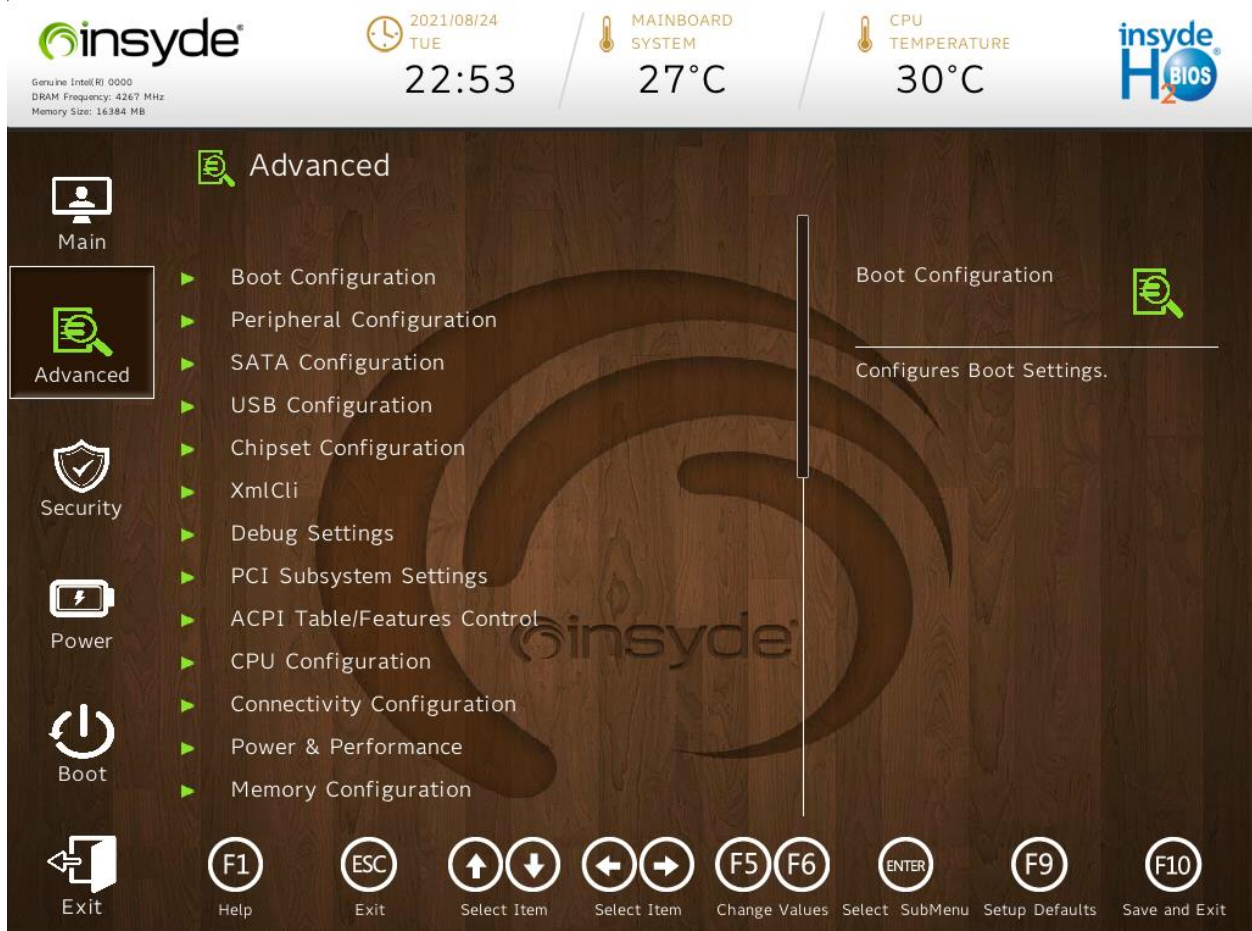
BIOS Setting	Options	Description
InsydeH2O Version	No options	Display the software version of the installed Insyde BIOS.
Processor Type	No options	Display the maker, model and speed of the installed CPU.
System Bus Speed	No options	Display the auto-detected speed of the System Bus.
System Memory Speed	No options	Display the auto-detected speed of the System Memory.
Cache RAM	No options	Display the current amount of Cache RAM in the system.
Total Memory	No options	Display the total amount of detected system memory installed in the system.
Controller0 Channel0 Row of chips0	No options	
Controller0 Channel1 Row of chips0	No options	
Controller0 Channel2 Row of chips0	No options	
Controller0 Channel3 Row of chips0	No options	
Controller1 Channel0 Row of chips0	No options	
Controller1 Channel1 Row of chips0	No options	
Controller1 Channel2 Row of chips0	No options	
Controller1 Channel3 Row of chips0	No options	
Platform Configuration		
CPUID	No options	Display the processor ID of the installed CPU.
CPU Speed	No options	Display the frequency of the CPU.
CPU Stepping	No options	
Core Information		
L1 Data Cache	No options	Display the size of the L1 cache for data usage.
L1 Instruction Cache	No options	Display the size of the L1 cache for instruction usage.
L2 Cache	No options	Display the size of the L2 cache.
L3 Cache	No options	Display the size of the L3 cache.
L4 Cache	No options	Display the size of the L4 cache.

Atom Core Information		
L1 Data Cache	No options	Display the size of the L1 cache for data usage.
L1 Instruction Cache	No options	Display the size of the L1 cache for instruction usage.
L2 Cache	No options	Display the size of the L2 cache.
L3 Cache	No options	Display the size of the L3 cache.
L4 Cache	No options	Display the size of the L4 cache.
Total Processor Count	No options	Display the number of all cores and all threads of the installed CPU.
Number Of Atom Core	No options	Display the number of atom cores and atom threads of the installed CPU.
Number Of Core	No options	Display the number of non-atom cores and non-atom threads of the installed CPU.
Microcode Rev	No options	The version of microcode.
GT Info	No options	The information of GT.
SMX/TXT	No options	Display the current platform support SMX/TXT or not.
PCH Rev / SKU	No options	Display the revision and SKU of PCH.
GOP Ver	No options	Display the current GOP version.
EC Ver	No options	Display the current EC version.
Board ID	No options	Display the name of the CRB.
FAB ID	No options	Display the revision of FAB.
Intel ME Version / SKU	No options	Display the current Intel ME version and SKU.
LAN PHY Revision	No options	Display the current LAN PHY.
Language	<b>[English]</b> [Français] [中文] [日本語]	Selects the current default language used by the InsydeH2O.
System Time	Adjust time	Allows user to change the time recognized by the system.
System Date	Adjust date	Allows user to change the date recognized by the system.
About this Software	No options	

## 2.2 Advanced Menu

Advanced Menu of InsydeH2O BIOS Setup Utility allows users to configure advanced system settings.

**Figure 2-2. Setup Utility Advanced Menu**



**Table 2-2. Advanced Menu Setting**

BIOS Setting	Options	Description
Boot Configuration	(See Section 2.2.1)	Configures Boot Settings.
Peripheral Configuration	(See Section 2.2.2)	Configures the peripheral devices.
SATA Configuration	(See Section 2.2.3)	Select the SATA controller and hard disk drive type installed in your system.
USB Configuration	(See Section 2.2.4)	Configures the USB support.
Chipset Configuration	(See Section 2.2.5)	Advanced Chipset Configuration Options.
XmlCli	(See Section 2.2.6)	BIOS XmlCli Setup Options.

Debug Settings	(See Section 2.2.7)	Debug interface Settings
PCI Subsystem Settings	(See Section 2.2.8)	PCI, PCI-X and PCI Express Settings.
ACPI Table/Features Control	(See Section 2.2.9)	Configures ACPI Tables/Features setting.
CPU Configuration	(See Section 2.2.10)	CPU Configuration.
Connectivity Configuration	(See Section 2.2.11)	Configures Connectivity related options.
Power & Performance	(See Section 2.2.12)	Power & Performance Options.
OverClocking Performance Menu	(See Section 2.2.13)	Performance Menu for Processor and Memory.
Memory Configuration	(See Section 2.2.14)	Memory Configuration Parameters.
System Agent (SA) Configuration	(See Section 2.2.15)	System Agent (SA) Parameters.
PCIE Configuration.	(See Section 2.2.16)	PCIE Parameters.
PCH-IO Configuration	(See Section 2.2.17)	PCH Parameters.
PCH-FW Configuration	(See Section 2.2.18)	Configures Management Engine Technology Parameters.
Thermal Configuration	(See Section 2.2.19)	Thermal Configuration Parameters.
Platform Settings	(See Section 2.2.20)	Platform related settings.
ACPI D3Cold settings	(See Section 2.2.21)	ACPI D3Cold related settings.
BCLK Configuration	(See Section 2.2.22)	BCLK Configuration options.

## 2.2.1 Boot Configuration

**Table 2-2-1. Boot Configuration**

BIOS Setting	Options	Description
Boot Configuration		
Numlock	<b>[OFF]</b> [ON]	Selects Power-on state for Numlock.

## 2.2.2 Peripheral Configuration

**Table 2-2-2. Peripheral Configuration**

BIOS Setting	Options	Description
Peripheral Configuration		
Serial Port A	<b>[Disable]</b>	Configure Serial port A using options :

	[Auto] [Enable]	[Disable] No Configuration [Enable] User Configuration [Auto] EFI/OS chooses configuration (Below options will show at this option set Enabled)
Base I/O Address	[2E8] [2F8] [3E8] [ <b>3F8</b> ]	Serial Port A Base IO Address. (show at Serial Port A set Enable)
Interrupt	[IRQ3] [ <b>IRQ4</b> ]	Serial Port A Interrupt (show at Serial Port A set Enable)
Infrared Port	[ <b>Disable</b> ] [Auto] [Enable]	Configure Infrared port using options : [Disable] No Configuration [Enable] User Configuration [Auto] EFI/OS chooses configuration
Mode	[ <b>CIR</b> ] [FIR]	Set the mode for the parallel port using options. (show at Infrared Port set Auto/Enable)
Base I/O Address	[2E8] [ <b>2F8</b> ] [3E8] [3F8]	Infrared Port Base IO Address. (Show at Infrared Port set Enable)
Interrupt	[ <b>IRQ3</b> ] [IRQ4]	Infrared Port Interrupt. (Show at Infrared Port set Enable)
DMA Channel	[DMA 1] [DMA 2] [ <b>DMA 3</b> ]	Infrared Port DMA Channel. (Show at Infrared Port set Enable)
High Speed	[ <b>Normal Speed</b> ] [High Speed]	Set FIR to High speed mode or normal speed mode. (Show at Infrared Port set Enable and Mode set FIR)

### 2.2.3 SATA Configuration

**Table 2-2-3. SATA Configuration**

BIOS Setting	Options	Description
SATA Configuration		
Serial ATA Port 0	[Not Installed]	Serial ATA Port 0 Device configuration
Serial ATA Port 1	[Not Installed]	Serial ATA Port 1 Device configuration
Serial ATA Port 2	[Not Installed]	Serial ATA Port 2 Device configuration
Serial ATA Port 3	[Not Installed]	Serial ATA Port 3 Device configuration
Serial ATA Port 6	[Not Installed]	Serial ATA Port 6 Device configuration
Serial ATA Port 7	[Not Installed]	Serial ATA Port 7 Device configuration

## 2.2.4 USB Configuration

**Table 2-2-4. USB Configuration**

BIOS Setting	Options	Description
USB Configuration		
USB BIOS Support	[Disable] <b>[Enable]</b>	USB keyboard/mouse/storage support under UEFI environment.
USB Legacy SMI bit Clean	<b>[Disable]</b> [Enable]	Clean Usb Legacy SMI bit for xHCI and EHCI

## 2.2.5 Chipset Configuration

**Table 2-2-5. Chipset Configuration**

BIOS Setting	Options	Description
Chipset Configuration		
Platform Trust Technology	<b>[Enable]</b> [Disable]	Enable/Disable Platform Trust Technology.

## 2.2.6 XmlCli

**Table 2-2-6. XmlCli**

BIOS Setting	Options	Description
XmlCli		

## 2.2.7 Debug Settings

**Table 2-2-7. Debug Settings**

BIOS Setting	Options	Description
Debug Settings		
Kernel Debug Serial Port	<b>[Legacy UART]</b> [SERIALIO UART0]	Select Kernel Debug Port and report in ACPI DBG2 table
Kernel Debug Patch	<b>[Disable]</b> [Enable]	Enable/Disable Kernel Debug Patch.
Platform Debug Consent	<b>[Disable]</b> [Enabled (All Probes+TraceHub)] [Enabled (Low Power)] [Manual]	Enabled(All Probes+TraceHub) supports all probes with TraceHub enabled and blocks s0ix\n\nEnabled(Low Power) Tracehub is powergated by default, s0ix is viable\n\nManual:user needs to configure Advanced Debug Settings manually, aimed at advanced users.
VT-d Debug Settings	(See Section 2.2.7.1)	
Advanced Debug Settings	(See Section 2.2.7.2)	

### 2.2.7.1 VT-d Debug Settings

**Table 2-2-7-1. VT-d Debug Settings**

BIOS Setting	Options	Description
VT-d Debug Settings		
IGD VTD Enable	<b>[Enable]</b> [Disable]	Enable/Disable IGD VTD.
IPU VTD Enable	<b>[Enable]</b> [Disable]	Enable/Disable IPU VTD.
IOP VTD Enable	<b>[Enable]</b> [Disable]	Enable/Disable IOP VTD.

### 2.2.7.2 Advanced Debug Settings

**Table 2-2-7-2. Advanced Debug Settings**

BIOS Setting	Options	Description
Advanced Debug Settings		
USB3 Type-C UFP2DFP Kernel/Platform Debug Support	[Disable] [Enable] <b>[No Change]</b>	This BIOS option enables kernel and platform debug for USB3 interface over a UFP Type-C receptacle, select 'No Change' will do nothing to UFP2DFP setting
USB Dbc Enable Mode	[Disabled] [USB2] [USB3] [Both] <b>[No Change]</b>	Disabled:Clear both USB2/3DBCEN. USB2:Set USB2DBCEN. USB3:Set USB3DBCEN. Both:Set both USB2/3DBCEN. No Change:Comply with HW value
DCI Enable	<b>[Disable]</b> [Enable]	Determine if to enable DCI debug from host. (Show as <u>Platform Debug Consent</u> is not Disable)
PCH Trace Hub Enable Mode	<b>[Disable]</b> [Target Debugger] [Host Debugger]	Select 'Host Debugger' if Trace Hub is used with host debugger tool or 'Target Debugger' if Trace Hub is used by target debugger software. Note: If 'Host Debugger' is selected, Platform Debug Consent has to be ENABLED because DCI is one of the primary trace data output paths.
PCH TH Mem Buffer Size 0	<b>[None/OS]</b> [1MB] [8MB] [64MB] [128MB] [256MB] [512MB]	Select size of memory region 0 buffer. Choose None/OS if OS-supported memory or trace forwarding is desired. Note : Limitation of total buffer size (PCH + CPU) is 512M (Show as <u>PCH Trace Hub Enable Mode</u> is not Disable)
PCH TH Mem Buffer Size 1	<b>[None/OS]</b> [1MB] [8MB] [64MB] [128MB] [256MB] [512MB]	Select size of memory region 1 buffer. Choose None/OS if OS-supported memory or trace forwarding is desired. Note : Limitation of total buffer size (PCH + CPU) is 512MB

		(Show as <u>PCH Trace Hub Enable Mode</u> is not Disable)
CPU Trace Hub Enable Mode	<b>[Disable]</b> [Target Debugger] [Host Debugger]	Select 'Target Debugger' if Trace Hub is used by target debugger software. Note: If 'Host Debugger' is selected, Platform Debug Consent has to be ENABLED because DCI is one of the primary trace data output paths.
CPU TH Mem Buffer Size 0	<b>[None/OS]</b> [1MB] [8MB] [64MB] [128MB] [256MB] [512MB]	Select size of memory region 0 buffer. Choose None/OS if OS-supported memory or trace forwarding is desired. Note : Limit of total buffer size (PCH + CPU) is 512MB when iTBT disabled, 256MB when iTBT enabled (Show as <u>PCH Trace Hub Enable Mode</u> is not Disable)
CPU TH Mem Buffer Size 1	<b>[None/OS]</b> [1MB] [8MB] [64MB] [128MB] [256MB] [512MB]	Select size of memory region 1 buffer. Choose None/OS if OS-supported memory or trace forwarding is desired. Note : Limit of total buffer size (PCH + CPU) is 512MB when iTBT disabled, 256MB when iTBT enabled (Show as <u>PCH Trace Hub Enable Mode</u> is not Disable)
CPU Run Control	[Disabled] [Enabled] <b>[No Change]</b>	Enable/Disable CPU Run Control Support; No Change : Comply with HW value
CPU Run Control Lock	[Disabled] <b>[Enabled]</b>	Enable/Disable CPU Run Control Lock (Show as <u>CPU Run Control</u> is not No Change)
USB Overcurrent Override for VISA	<b>[Disable]</b> [Enable]	This option overrides USB Over Current enablement state that USB OC will be disabled after enabling this option. Enable when VISA pin is muxed with USB OC.
Processor trace memory allocation	<b>[Disable]</b> [4KB] [8KB] [16KB] [32KB] [64KB] [128KB] [256KB] [512KB] [1MB] [2MB] [4MB] [8MB] [16MB] [32MB] [64MB] [128MB]	Disable or Select Processor trace memory region Size: from 4KB ~ 128MB (Show as <u>SETUP_CPU_FEATURES.ProcTraceSupported</u> is not 0;)
Processor trace	<b>[Disable]</b> [Enable]	Enable/Disable processor trace feature from CPU MSR. Enabling this feature will immediately start trace collection. (Show as <u>SETUP_CPU_FEATURES.ProcTraceSupported</u> is not 0; OR <u>CPU_SETUP.ProcessorTraceMemSize</u> is not 0xFF;)
Processor Trace OutPut Scheme	<b>[Single Range Output]</b> [ToPA Output]	Select Single Range Output scheme or ToPA table Output scheme. (Show as <u>SETUP_CPU_FEATURES.ProcTraceSupported</u> is

		not 0; OR <i>CPU_SETUP.ProcessorTraceMemSize</i> is not 0xFF;)
JTAG C10 Power Gate	[Disable] <b>[Enable]</b>	When Enabled, JTAG is power gated in C10 state. When Disabled, keeps the JTAG power up during C10 and deeper power states for debug purpose.
Three Strike Counter	[Disable] <b>[Enable]</b>	Enable/Disable Three Strike Counter.
CrashLog Feature	[Disable] <b>[Enable]</b>	The feature helps collecting crash data from PMC SSRAM.
CrashLog On All Reset	<b>[Disable]</b> [Enable]	Option to invoke CrashLog collection on all reset.
CrashLog Rearm Enable	[Disable] <b>[Enable]</b>	Option to invoke crashLog re-arm.
CrashLog Clear Enable	<b>[Disable]</b> [Enable]	Option to invoke CrashLog clear
CrashLog GPRs	<b>[Disable]</b> [Enable] [Gprs Enabled, Smm Gprs Disabled]	Helps collecting crash data from PMC SSRAM. Enabling this may expose personal or confidential information that may be held in the GPRs at the time of the Crash trigger.
PMC Debug Message Enable	<b>[Disable]</b> [Enable]	When Enabled, PMC HW will send debug messages to trace hub; When Disabled, PMC HW will never send debug messages to trace hub. Noted: When Enabled, may not enter S0ix
Delayed Authentication Mode	[Disable] <b>[Enable]</b>	Enable/Disable Delayed Authentication Mode. Enabled if debug consent is enabled. (Show as <i>ME_SETUP.STORAGE.AfterEoP</i> is not 0x1)

## 2.2.8 PCI Subsystem Settings

**Table 2-2-8. PCI Subsystem Settings**

BIOS Setting	Options	Description
PCI Subsystem Settings		
PCI Bus Driver Version	No options	PCI, PCI-X and PCI Express Settings.
PCI ROM Priority	[Legacy ROM] <b>[EFI Compatible ROM]</b>	In case of multiple Option ROMs (Legacy and EFI Compatible), specifies what PCI Option rom to launch.
External DMA Allowed On Boot	<b>[No]</b> [Yes]	External DMA Allowed On Boot for devices such as 1394, PCMCIA, & CardBus.
Install Ext OpRom Before BIOS Setup	<b>[Disable]</b> [Ext PCIE Storage OpRom]	Install Ext OpRom for Storage or Other device before BIOS Setup, That we

	[Ext PCIE Other OpRom] [Ext PCIE Both Storage and Other OpRom]	can get the Ext PCIE Card OpRom Setup Menu and have chance to enter into it.
PCI Latency Timer	<b>[32 PCI Bus Clocks]</b> [64 PCI Bus Clocks] [96 PCI Bus Clocks] [128 PCI Bus Clocks] [160 PCI Bus Clocks] [192 PCI Bus Clocks] [224 PCI Bus Clocks] [248 PCI Bus Clocks]	Value to be programmed into PCI Latency Timer Register.

## 2.2.9 ACPI Table/Features Control

**Table 2-2-9. ACPI Table/Features Control**

BIOS Setting	Options	Description
ACPI Table/Features Control		
ACPI Settings	(See Section 2.2.9.1)	System ACPI Parameters
FACP - RTC S4 Wakeup	[Disable] <b>[Enable]</b>	Value only for ACPI. Enable/Disable for S4 Wakeup from RTC
APIC - IO APIC Mode	[Disable] <b>[Enable]</b>	This item is valid only for WIN2k and WINXP. Also, a fresh install of the OS must occur when APIC Mode is desired. Test the IO ACPI by setting item to Enable. The APIC Table will then be pointed to by the RSDT, the Local APIC will be initialized, and the proper enable bits will be set in ICH4M

### 2.2.9.1 ACPI Settings

**Table 2-2-9-1. ACPI Settings**

BIOS Setting	Options	Description
ACPI Settings		
ACPI Version	No options	ACPI Version details
Enable ACPI Auto Configuration	<b>[Disable]</b> [Enable]	Enables or Disables BIOS ACPI Auto Configuration.
Enable Hibernation	[Disable] <b>[Enable]</b>	Enables or Disables System ability to Hibernate (OS/S4 Sleep State). This option may not be effective with some OSs. (Show as <u>Enable ACPI Auto Configuration</u> is not Enable)
PTID Support	[Disable] <b>[Enable]</b>	PTID Support will be loaded if enabled. (Show as <u>Enable ACPI Auto Configuration</u> is not Enable)

PECI Access Method	<b>[Direct I/O]</b> [ACPI]	PECI Access Method is Direct I/O or ACPI (Show as <u>Enable ACPI Auto Configuration</u> is not Enable)
ACPI S3 Support	[Disabled] <b>[Enabled]</b>	ACPI S3 Support (Show as <u>Enable ACPI Auto Configuration</u> is not Enable)
Native PCIE Enable	[Disabled] <b>[Enabled]</b>	Bit - PCIE Native * control 0 - ~ Hot Plug 1 - SHPC Native Hot Plug control 2 - ~ Power Management Events 3 - PCIE Advanced Error Reporting control 4 - PCIE Capability Structure control 5 - Latency Tolerance Reporting control (Show as <u>PCH_SETUP.PcieRootPortEn[OFFSET_0]</u> is not 0x0)
Native ASPM	<b>[Auto]</b> [Enabled] [Disabled]	Enabled - OS Controlled ASPM, Disabled - BIOS Controlled ASPM (Show as <u>Native PCIE Enable</u> is not Disable)
Wake System from S5 via RTC	<b>[Disabled]</b> [Enabled]	Enable or disable System wake on alarm event. When enabled, System will wake on the hr::min::sec specified. (Show as RTCWakeup_SUPPORT_FLAG is defined)
Wake up hour	<b>minimum = 0</b> <b>maximum = 23</b> <b>step = 1</b> <b>default = 0</b>	select 0-23 For example enter 3 for 3am and 15 for 3pm
Wake up minute	<b>minimum = 0</b> <b>maximum = 59</b> <b>step = 1</b> <b>default = 0</b>	0 - 59
Wake up second	<b>minimum = 0</b> <b>maximum = 59</b> <b>step = 1</b> <b>default = 0</b>	0 - 59
BDAT ACPI Table Support	<b>[Disabled]</b> [Enabled]	Enables support for the BDAT ACPI table.
ACPI Debug	<b>[Disabled]</b> [Enabled]	Open a memory buffer for storing debug strings. Reenter SETUP after enabling to see the buffer address. Use method ADBG to write strings to buffer. (Below options will show at this option set <u>Enabled</u> )
Acpi Memory Buffer Address	No options	Acpi Memory Buffer Address.
Print to Serial Port	<b>[Disabled]</b> [Enabled]	Print copy of ACPI debug logs to serial port.

Whea Driver Support	<b>[Disabled]</b> [Enabled]	Enables or Disables Whea Driver Support. This option may be not effective with some OS. (Show as WHEA_SUPPORT_FLAG is defined)
Log Errors	<b>[Disabled]</b> [Enabled]	(Show as WHEA_SUPPORT_FLAG is defined)
Error Generation	[NoInband] <b>[SMI/PMI]</b>	IIO Error Generation. (Show as WHEA_SUPPORT_FLAG is defined)
PCH Errors	[No] <b>[Yes]</b>	(Show as WHEA_SUPPORT_FLAG is defined)
PCI-Ex Errors	[No] <b>[Yes]</b>	(Show as WHEA_SUPPORT_FLAG is defined)
Platform Errors	<b>[No]</b> [Yes]	(Show as WHEA_SUPPORT_FLAG is defined)
Enable SERR propagation	[No] <b>[Yes]</b>	(Show as WHEA_SUPPORT_FLAG is defined)
Enable PERR propagation	[No] <b>[Yes]</b>	(Show as WHEA_SUPPORT_FLAG is defined and (WHEA_SETUP.LogErrors is not 0 OR WHEA_SETUP.PropagateSerr is not 0))
Fatal Errors	<b>[Disabled]</b> [Enabled]	Enable & escalate fatal errors to error pins. (Show as WHEA_SUPPORT_FLAG is defined and (WHEA_SETUP.LogErrors is not 0 OR WHEA_SETUP.PcieErrors is not 0))
Uncorrectable/Recoverable Non Fatal Errors	<b>[Disabled]</b> [Enabled]	Enable & escalate Uncorrectable/Recoverable to error pins. (Show as WHEA_SUPPORT_FLAG is defined)
Correctable Errors	<b>[Disabled]</b> [Enabled]	Enable & escalate Correctable Errors to error pins. (Show as WHEA_SUPPORT_FLAG is defined)
Low Power S0 Idle Capability	[Disabled] <b>[Enabled]</b>	This variable determines if we enable ACPI Lower Power S0 Idle Capability (Mutually exclusive with Smart connect). While this is enabled, it also disable 8254 timer for SLP_S0 support.
PUIS Enable	[Enabled] <b>[Disabled]</b>	Enable/Disable Power-Up In Standby (PUIS) feature set allows devices to be powered-up into the Standby power management state to minimize inrush current at power-up and to allow the host to sequence the spin-up of devices. (Show as <u>SETUP_VOLATILE_DATA.PlatformFlavor</u> is FlavorDesktop)
EC Notification	[Disabled] <b>[Enabled]</b>	Sends EC notification of Low Power S0 Idle State (Show as <u>SETUP_DATA.LowPowerS0Idle</u> is 1)
EC CS Debug Light	<b>[Disabled]</b> [Enabled]	When EC enters Low Power S0 Idle State, the CAPS LOCK light will be turned on (Show as <u>SETUP_DATA.CSNotifyEC</u> is 1)

EC Low Power Mode	[Disabled] <b>[Enabled]</b>	This option controls whether EC will go to Low power mode during Low Power S0 Idle State (Show as <u>SETUP_DATA.NoEcLowPowerExitGpio</u> is not 1)
Sensor Standby	<b>[Disabled]</b> [Enabled]	Enable/Disable Sensor standby mode
CS PL1 Limit	<b>[Disabled]</b> [Enabled]	Limit PL1 (Power Limit 1) while in Connected Standby
CS PL1 Value	<b>minimum = 3000</b> <b>maximum = 20000</b> <b>step = 125</b> <b>default = 4500</b>	PL1 value is in milliwatts with 125 step value (Show as <u>CS PL1 Limit</u> set to Enable)
PEP Constraints Configuration	(See Section 2.2.9.1.1)	Control which controllers get included in PEP constraint list
LPIT Residency Counter	[C10] <b>[SLP S0]</b>	Select Residency Counter
SSDT table from file	<b>[Disabled]</b> [Enabled]	SSDT table from file.
PCI Delay Optimization	<b>[Disabled]</b> [Enabled]	Experimental ACPI additions for FW latency optimizations.
MSI enabled	[Disabled] <b>[Enabled]</b>	When disabled, MSI support is disabled in FADT.

### 2.2.9.1.1 PEP Constraints Configuration

**Table 2-2-9-1-1. PEP Constraints Configuration**

BIOS Setting	Options	Description
PEP Constraints Configuration		
PEP CPU	[Disabled] <b>[Enabled]</b>	Add CPU in PEP mitigation list
PEP Graphics	[Disabled] <b>[Enabled]</b>	Add Gfx in PEP mitigation list
PEP IPU	[Disabled] <b>[Enabled]</b>	Add IPU in PEP mitigation list
PEP GNA	[Disabled] <b>[Enabled]</b>	Add GNA in PEP mitigation list
PEP SATA	[No Constraint] [Adapter D0/F1] [Raid Volume0] <b>[Adapter D3]</b>	Add Storage device in PEP mitigation list
PEP enumerated SATA ports	<b>[Disabled]</b> [Enabled]	Add enumerated SATA ports in PEP Constraint list
PEP PCIe Storage	[No Constraint] [D0/F1] <b>[D3]</b>	Add PCIe root ports (storage) in PEP mitigation list

PEP PCIe LAN	[No Constraint] <b>[D0/F1]</b> [D3]	Add PCIe root ports (LAN) in PEP mitigation list
PEP PCIe WLAN	[No Constraint] <b>[D0/F1]</b> [D3]	Add PCIe root ports (WLAN) in PEP mitigation list
PEP PCIe GFX	[No Constraint] <b>[D0/F1]</b> [D3]	Add PCIe root ports (GFX) in PEP mitigation list
PEP PCIe Other	<b>[No Constraint]</b> [D0/F1] [D3]	Add PCIe root ports (Other) in PEP mitigation list
PEP PCIe DG	[Disabled] <b>[Enabled]</b>	Add PCIe DG PEP Constraint
PEP UART	[Disabled] <b>[Enabled]</b>	Add UART in PEP mitigation list
PEP I2C0	[Disabled] <b>[Enabled]</b>	Adds I2C in PEP mitigation list
PEP I2C1	[Disabled] <b>[Enabled]</b>	Adds I2C in PEP mitigation list
PEP I2C2	[Disabled] <b>[Enabled]</b>	Adds I2C in PEP mitigation list
PEP I2C3	[Disabled] <b>[Enabled]</b>	Adds I2C in PEP mitigation list
PEP I2C4	[Disabled] <b>[Enabled]</b>	Adds I2C in PEP mitigation list
PEP I2C5	[Disabled] <b>[Enabled]</b>	Adds I2C in PEP mitigation list
PEP I2C6	[Disabled] <b>[Enabled]</b>	Adds I2C in PEP mitigation list
PEP I2C7	[Disabled] <b>[Enabled]</b>	Adds I2C in PEP mitigation list
PEP SPI	[Disabled] <b>[Enabled]</b>	Add SPI in PEP mitigation list
PEP XHCI	[Disabled] <b>[Enabled]</b>	Add XHCI in PEP mitigation list
PEP Audio	[No Constraint] <b>[D0/F1]</b> [D3]	Add Audio in PEP mitigation list (This options can be set at HD Audio set Enabled.)
PEP CSME	[Disabled] <b>[Enabled]</b>	Add CSME in PEP mitigation list
PEP HECI3	[Disabled] <b>[Enabled]</b>	Add HECI3 in PEP mitigation list
PEP LAN(GBE)	[Disabled] <b>[Enabled]</b>	Add LAN(GBE) in PEP mitigation list (This options can be set at PCH LAN Controller set Enabled.) (Show as <u>SETUP_VOLATILE_DATA.GbeAvailable</u> is not 0 )
PEP THC0	[Disabled] <b>[Enabled]</b>	Add THC in PEP mitigation list. Applies only if THCx has assigned port
PEP THC1	[Disabled] <b>[Enabled]</b>	Add THC in PEP mitigation list. Applies only if THCx has assigned port

PEP UFS0	[Disabled] <b>[Enabled]</b>	Add UFS0 IPs in PEP mitigation list
PEP UFS1	[Disabled] <b>[Enabled]</b>	Add UFS1 IPs in PEP mitigation list
PEP TCSS	[Disabled] <b>[Enabled]</b>	Add TCSS IPs in PEP mitigation list
PEP VMD	[Disabled] <b>[Enabled]</b>	Add VMD in PEP mitigation list

## 2.2.10 CPU Configuration

**Table 2-2-10. CPU Configuration**

BIOS Setting	Options	Description
Core Information	No options	Displays the Core Information.
ID	No options	Displays the Processor ID.
Brand String	No options	Brand String of the Performance Processor
VMX	No options	VMX Supported or Not
SMX/TXT	No options	SMX/TXT Supported or Not
TXT Crash Code	No options	TXT Crash Code Register value
TXT SPAD	No options	TXT SPAD Register value
Boot Guard Status	No options	Boot Guard Status Register value
Boot Guard ACM Policy Status	No options	Boot Guard ACM Policy Status value
Boot Guard SACM Information	No options	Boot Guard SACM Info MSR value
C6DRAM	[Disabled] <b>[Enabled]</b>	Enable/Disable moving of DRAM contents to PRM memory when CPU is in C6 state (Show as <i>SETUP_CPU_FEATURES.C6DramSupported</i> is not 0 )
CPU Flex Ratio Override	[Disabled] <b>[Enabled]</b>	Enable/Disable CPU Flex Ratio Programming (Below options can be set at this option set <u>Enabled</u> )
CPU Flex Ratio Settings	<b>minimum = 0</b> <b>maximum = 63</b> <b>step = 0</b> <b>default = 20</b>	This value must be between Max Efficiency Ratio (LFM) and Maximum non-turbo ratio set by Hardware (HFM).
Hardware Prefetcher	[Disabled] <b>[Enabled]</b>	To turn on/off the MLC streamer prefetcher.
Adjacent Cache Line Prefetch	[Disabled] <b>[Enabled]</b>	To turn on/off prefetching of adjacent cache lines.

Intel (VMX) Virtualization Technology	[Disabled] <b>[Enabled]</b>	When enabled, a VMM can utilize the additional hardware capabilities provided by Vanderpool Technology. (Show as <u>SETUP_CPU_FEATURES.VTAvailable</u> is not 0)
PECI	[Disabled] <b>[Enabled]</b>	Enable/Disable PEFI
AVX	<b>[Enabled]</b> [Disabled]	Enable/Disable the AVX 2 Instructions. This is applicable for Big Core only.
Active Cores	<b>[All]</b> [0] [1] [2] [3] [4] [5] [6] [7] [8]	Number of cores to enable in each processor package. Note: Number of Cores and AtomCores are looked at together. When both are {0,0}, Pcode will enable all cores.
Active Atom Cores	<b>[All]</b> [0] [1] [2] [3] [4] [5] [6] [7] [8]	Number of atom cores to enable in each processor package. Note: Number of Cores and AtomCores are looked at together. When both are {0,0}, Pcode will enable all cores.
Hyper-Threading	[Disabled] <b>[Enabled]</b>	Enable or Disable Hyper-Threading Technology. (Show as <u>SETUP_CPU_FEATURES.HTAvailable</u> is not 1)
BIST	<b>[Disabled]</b> [Enabled]	Enable/Disable BIST (Built-In Self Test) on reset.
AP threads Idle Manner	[HALT Loop] <b>[MWAIT Loop]</b> [RUN Loop]	AP threads Idle Manner for waiting signal to run. (MWAIT Loop will show at <u>MonitorMwait</u> set Enabled.)
AES	[Disabled] <b>[Enabled]</b>	Enable/Disable AES (Advanced Encryption Standard) (Show as <u>SETUP_CPU_FEATURES.AESAvailable</u> is not 0)
MachineCheck	[Disabled] <b>[Enabled]</b>	Enable/Disable Machine Check
MonitorMWait	[Disabled] <b>[Enabled]</b>	Enable/Disable MonitorMWait, if Disable MonitorMwait, the AP threads Idle Manner should not set in MWAIT Loop
Intel Trusted Execution Technology	<b>[Disabled]</b> [Enabled]	Enables utilization of additional hardware capabilities provided by Intel (R) Trusted Execution Technology. Changes require a full power cycle to take effect. (Show as PcdTXTSupported is true, <u>SETUP_CPU_FEATURES.TXTAvailable</u> is not 0 OR <u>(SystemConfig.TpmDeviceOk</u> is not 0 AND <u>SystemConfig.Tpm2DeviceOk</u> is not 0) OR

		<i>SA_SETUP.EnableVtd</i> is not 0 OR <i>CPU_SETUP.ActiveCoreCount</i> is 0 OR ( <i>CPU_SETUP.HyperThreading</i> is not 0 AND <i>SETUP_CPU_FEATURES.HTAvailable</i> is not 1))
Alias Check Request	<b>[Disabled]</b> [Enabled]	Enables Txt Alias Checking capability Changes require full Txt capability before it will take effect. It is a one time only change, next reboot will be reset.
DPR Memory Size (MB)	<b>minimum = 0</b> <b>maximum = 255</b> <b>step = 1</b> <b>default = 4</b>	Reserve DPR memory size (0-255) MB
Reset AUX Content	[Yes] <b>[no]</b>	Reset TPM Aux content. Txt may not functional after AUX content gets reset.
BIOS Guard	No options	BIOS Guard
Enable Tools Interface	[Disabled] <b>[Enabled]</b>	Configure Tools Interface. Options are: <b>DISABLE</b> - Disable Tools Interface; <b>ENABLE</b> - Enable Tools Interface.
CPU SMM Enhancement	No options	CPU SMM Enhancement
SMM Use Delay Indication	[Disabled] <b>[Enabled]</b>	Enable/Disable usage of SMM_DELAYED MSR for MP sync in SMI
SMM Use Block Indication	[Disabled] <b>[Enabled]</b>	Enable/Disable usage of SMM_BLOCKED MSR for MP sync in SMI
SMM Use en-US Indication	[Disabled] <b>[Enabled]</b>	Enable/Disable usage of SMM_ENABLE MSR for MP sync in SMI
Total Memory Encryption	<b>[Disabled]</b> [Enabled]	Configure Total Memory Encryption (TME) to protect DRAM data from physical attacks.

## 2.2.11 Connectivity Configuration

**Table 2-2-11. Connectivity Configuration**

BIOS Setting	Options	Description
CNVi CRF present	No	[Yes] means CNVi is the active Connectivity Solution, [No] means CNVi was not discovered
CNVi Configuration	No options	CNVi Configuration
CNVi Mode	[Disable Integrated] <b>[Auto Detection]</b>	This option configures Connectivity. [Auto Detection] means that if Discrete solution is discovered it will be enabled

		<p>by default. Otherwise Integrated solution (CNVi) will be enabled; [Disable Integrated] disables Integrated Solution.</p> <p>NOTE: When CNVi is present, the GPIO pins that are used for radio interface cannot be assigned to the other native function.</p> <p><u>(Below options will show at this option set Auto Detection)</u></p>
Wi-Fi Core	<b>[Enabled]</b> [Disabled]	<p>This is an option intended to Enable/Disable Wi-Fi Core in CNVi (Show as stringref <u>STR_CNVI_IS_NOT_PRESENT_PATTERN</u> doesn't match <u>STR_CNVI_CURRENT_STATE</u>)</p>
BT Core	<b>[Enabled]</b> [Disabled]	<p>This is an option intended to Enable/Disable BT Core in CNVi (Below options can be set at this option set Enabled) (Show as stringref <u>STR_CNVI_IS_NOT_PRESENT_PATTERN</u> doesn't match <u>STR_CNVI_CURRENT_STATE</u>)</p>
BT Audio Offload	<b>[Enabled]</b> [Disabled]	<p>This is an option to Enable/Disable BT Audio Offload which enables audio input from BT device in HFP format to the audio DSP and enables power efficient audio output to BT device via A2DP format. This feature only support with Intel(R) Wireless-AX 22560 (Show as stringref <u>STR_CNVI_IS_NOT_PRESENT_PATTERN</u> doesn't match <u>STR_CNVI_CURRENT_STATE</u>)</p>
RFI Mitigation	<b>[Enabled]</b> [Disabled]	<p>This is an option intended to Enable/Disable DDR-RFIM feature</p>
CoExistence Manager	<b>[Disabled]</b> [Enabled]	<p>CoEx Manager mitigates radio coexistence issues between Intel WWAN (modem) and Intel WLAN (WiFi/BT). This should be enabled only if both WWAN and WLAN solutions are based on Intel components (Show as <u>SETUP_DATA.WwanEnable</u> is not 0)</p>
Preboot BLE	<b>[Disabled]</b> [Enabled]	<p>This will be used to enable Preboot Bluetooth function.</p>

		(Below options will show at this option set Enabled)
Discrete Bluetooth Interface	[Disabled] <b>[USB]</b> [UART]	SerialIo UART0 needs to be enabled to select BT interface (Below options will show at this option set Thunder Peak)
BT Interrupt Mode	<b>[GPIO Interrupt]</b> [APIC Interrupt]	Selects routing of interrupt from BT Module
BT Tile Mode	<b>[Disabled]</b> [Enabled]	Enable/Disable Tile
Tile S0	<b>minimum = 0</b> <b>maximum = 7</b> <b>step = 1</b> <b>default = 0</b>	The activity of Tile in S0.\nBit0:Find My PC\nBit1:Ring Notification\nBit2:BT_LED# Signal
Tile S0ix	<b>minimum = 0</b> <b>maximum = 7</b> <b>step = 1</b> <b>default = 0</b>	The activity of Tile in S0ix.\nBit0:Find My PC\nBit1:Ring Notification\nBit2:BT_LED# Signal
Tile S4	<b>minimum = 0</b> <b>maximum = 7</b> <b>step = 1</b> <b>default = 0</b>	The activity of Tile in S4.\nBit0:Find My PC\nBit1:Ring Notification\nBit2:BT_LED# Signal
Tile S5	<b>minimum = 0</b> <b>maximum = 7</b> <b>step = 1</b> <b>default = 0</b>	The activity of Tile in S5.\nBit0:Find My PC\nBit1:Ring Notification\nBit2:BT_LED# Signal
BT LED Config	<b>minimum = 0</b> <b>maximum = 3</b> <b>step = 1</b> <b>default = 0</b>	BT LED Config\nBit0:Define LED to Tile Ring Notification\nBit1:Active High Polarity
BT LED Pulse Duration	<b>minimum = 1</b> <b>maximum = 0xFF</b> <b>step = 1</b> <b>default = 1</b>	LED Duration in milliseconds.\nMin: 1ms\nMax: 1000ms
BT LED Pulse Interval	<b>minimum = 10</b> <b>maximum = 0xFF</b> <b>step = 10</b> <b>default = 10</b>	LED Pulse interval in tens of milliseconds.\nMin: 10ms\nMax: 255ms
Advanced settings	<b>[Disabled]</b> [Enabled]	Configure ACPI objects for wireless devices (Below options will show at this option set Enabled)
Switched Antenna Diversity Selection	[Antenna1] [Antenna2] <b>[Diversity]</b> [Diversity Antenna1] [Diversity Antenna2]	This allows WiFi modules which have only one antenna to use one of the 2 possible antennas with the options: 0 - Antenna1 1 - Antenna2 2 - Diversity 3 - Diversity Antenna1 4 - Diversity Antenna2

SPLC	No Options	SPLC
Domain Type SPLC 1	<b>minimum = 0</b> <b>maximum = 0x14</b> <b>step = 1</b> <b>default = 0x7</b>	09h: Module; 07h: WiFi/WLAN; 0Fh: WWAN; 10h: WiGig; 14h: RFEM
Default Power Limit	<b>minimum = 1</b> <b>maximum = 0xFFFF</b> <b>step = 1</b> <b>default = 0xFFFF</b>	Power Limit in milliwatts; Values between 10000 and 65535 will be treated as 65535
Default Time Window	<b>minimum = 1</b> <b>maximum = 100000</b> <b>step = 1</b> <b>default = 30000</b>	Time Window in milli seconds
WAND	No Options	WAND
TRxDelay_A	<b>minimum = 1</b> <b>maximum = 100</b> <b>step = 1</b> <b>default = 50</b>	Antenna A delay possible values: 1-100 in 10ths of nano seconds resolution
TRxCableLength_A	<b>minimum = 1</b> <b>maximum = 100</b> <b>step = 1</b> <b>default = 50</b>	Antenna A cable length possible values: 1-100cm in 1cm resolution
TRxDelay_B	<b>minimum = 1</b> <b>maximum = 100</b> <b>step = 1</b> <b>default = 50</b>	Antenna B delay possible values: 1-100 in 10ths of nano seconds resolution
TRxCableLength_B	<b>minimum = 1</b> <b>maximum = 100</b> <b>step = 1</b> <b>default = 50</b>	Antenna B cable length possible values: 1-100cm in 1cm resolution
WRDD Package 1	No options	WRDD Package 1
Domain Type	<b>minimum = 0</b> <b>maximum = 100</b> <b>step = 1</b> <b>default = 0x07</b>	09h: Module; 07h: WiFi/WLAN; 0Fh: WWAN; 10h WiGig; 14h: RFEM
Country Identifier	<b>minimum = 1</b> <b>maximum = 0xFFFF</b> <b>step = 1</b> <b>default = 0x4150</b>	Country identifier as defined in ISO/IEC 3166-1 Alpha 2 code
11Ax Control	No options	11Ax Control
11Ax Setting for UKraine	<b>[Disabled]</b> [Enable]	11Ax Setting for Ukraine Bit 0 - Apply changes to country Ukraine. 11Ax Setting within module certification 00 - None. Work with Wi-Fi FW/OTP

		definitions [Default]\n01 - Apply changes
11Ax Mode for Ukraine	<b>[Disabled]</b> [Enable]	11Ax Mode for Ukraine\nBit 1 - 11Ax Mode. Effective only if Bit 0 set to 1\n00 - Disable 11Ax on country Ukraine [Default]\n01 - Enable 11Ax on country Ukraine
11Ax Setting for Russia	<b>[Disabled]</b> [Enable]	11Ax Setting for Russia\nBit 2 - Apply changes to country Russia. 11Ax Setting within module certification\n00 - None. Work with Wi-Fi FW/OTP definitions [Default]\n01 - Apply changes
11Ax Mode for Russia	<b>[Disabled]</b> [Enable]	11Ax Mode for Russia\nBit 3 - 11Ax Mode. Effective only if Bit 2 set to 1\n00 - Disable 11Ax on country Russia [Default]\n01 - Enable 11Ax on country Russia
WRDS Package	No options	WRDS Package
WiFi SAR	<b>[Disabled]</b> [Enabled]	Enable/Disable WiFi SAR Tx Power Limit; DISABLE - Device ignores WiFi SAR Configuration Table; ENABLE - Device uses WiFi SAR Configuration Table <u>(Below options will show at this option set Enabled)</u>
SAR 2400 MHz Set1 Chain A	<b>minimum = 0</b> <b>maximum = 0xFF</b> <b>step = 1</b> <b>default = 0</b>	Defines the WiFi SAR Tx Power Limit - 8bit unsigned with 5bit integer and 3bit fractional. 0x00 = 0b00000000 = 0.125dB; 0xFF = 0b11111111 = 31.875dB. Each step is equivalent to 0.125dB
SAR 5150-5350 MHz Set1 Chain A	<b>minimum = 0</b> <b>maximum = 0xFF</b> <b>step = 1</b> <b>default = 0</b>	Defines the WiFi SAR Tx Power Limit - 8bit unsigned with 5bit integer and 3bit fractional. 0x00 = 0b00000000 = 0.125dB; 0xFF = 0b11111111 = 31.875dB. Each step is equivalent to 0.125dB
SAR 5350-5470 MHz Set1 Chain A	<b>minimum = 0</b> <b>maximum = 0xFF</b> <b>step = 1</b> <b>default = 0</b>	Defines the WiFi SAR Tx Power Limit - 8bit unsigned with 5bit integer and 3bit fractional. 0x00 = 0b00000000 = 0.125dB; 0xFF = 0b11111111 = 31.875dB. Each step is equivalent to 0.125dB
SAR 5470-5725 MHz Set1 Chain A	<b>minimum = 0</b> <b>maximum = 0xFF</b> <b>step = 1</b> <b>default = 0</b>	Defines the WiFi SAR Tx Power Limit - 8bit unsigned with 5bit integer and 3bit fractional. 0x00 = 0b00000000 = 0.125dB; 0xFF = 0b11111111 = 31.875dB. Each step is equivalent to 0.125dB

SAR 5725-5925 MHz Set1 Chain A	<b>minimum = 0</b> <b>maximum = 0xFF</b> <b>step = 1</b> <b>default = 0</b>	Defines the WiFi SAR Tx Power Limit - 8bit unsigned with 5bit integer and 3bit fractional. 0x00 = 0b00000000 = 0.125dB; 0xFF = 0b11111111 = 31.875dB. Each step is equivalent to 0.125dB
SAR 5945-6165 MHz Set1 Chain A	<b>minimum = 0</b> <b>maximum = 0xFF</b> <b>step = 1</b> <b>default = 0</b>	Defines the WiFi SAR Tx Power Limit - 8bit unsigned with 5bit integer and 3bit fractional. 0x00 = 0b00000000 = 0.125dB; 0xFF = 0b11111111 = 31.875dB. Each step is equivalent to 0.125dB
SAR 6165-6405 MHz Set1 Chain A	<b>minimum = 0</b> <b>maximum = 0xFF</b> <b>step = 1</b> <b>default = 0</b>	Defines the WiFi SAR Tx Power Limit - 8bit unsigned with 5bit integer and 3bit fractional. 0x00 = 0b00000000 = 0.125dB; 0xFF = 0b11111111 = 31.875dB. Each step is equivalent to 0.125dB
SAR 6405-6525 MHz Set1 Chain A	<b>minimum = 0</b> <b>maximum = 0xFF</b> <b>step = 1</b> <b>default = 0</b>	Defines the WiFi SAR Tx Power Limit - 8bit unsigned with 5bit integer and 3bit fractional. 0x00 = 0b00000000 = 0.125dB; 0xFF = 0b11111111 = 31.875dB. Each step is equivalent to 0.125dB
SAR 6525-6705 MHz Set1 Chain A	<b>minimum = 0</b> <b>maximum = 0xFF</b> <b>step = 1</b> <b>default = 0</b>	Defines the WiFi SAR Tx Power Limit - 8bit unsigned with 5bit integer and 3bit fractional. 0x00 = 0b00000000 = 0.125dB; 0xFF = 0b11111111 = 31.875dB. Each step is equivalent to 0.125dB
SAR 6705-6865 MHz Set1 Chain A	<b>minimum = 0</b> <b>maximum = 0xFF</b> <b>step = 1</b> <b>default = 0</b>	Defines the WiFi SAR Tx Power Limit - 8bit unsigned with 5bit integer and 3bit fractional. 0x00 = 0b00000000 = 0.125dB; 0xFF = 0b11111111 = 31.875dB. Each step is equivalent to 0.125dB
SAR 6865-7105 MHz Set1 Chain A	<b>minimum = 0</b> <b>maximum = 0xFF</b> <b>step = 1</b> <b>default = 0</b>	Defines the WiFi SAR Tx Power Limit - 8bit unsigned with 5bit integer and 3bit fractional. 0x00 = 0b00000000 = 0.125dB; 0xFF = 0b11111111 = 31.875dB. Each step is equivalent to 0.125dB
SAR 2400 MHz Set1 Chain B	<b>minimum = 0</b> <b>maximum = 0xFF</b> <b>step = 1</b> <b>default = 0</b>	Defines the WiFi SAR Tx Power Limit - 8bit unsigned with 5bit integer and 3bit fractional. 0x00 = 0b00000000 = 0.125dB; 0xFF = 0b11111111 = 31.875dB. Each step is equivalent to 0.125dB
SAR 5150-5350 MHz Set1 Chain B	<b>minimum = 0</b> <b>maximum = 0xFF</b>	Defines the WiFi SAR Tx Power Limit - 8bit unsigned with 5bit integer and 3bit

	<b>step = 1</b> <b>default = 0</b>	fractional. 0x00 = 0b00000000 = 0.125dB; 0xFF = 0b11111111 = 31.875dB. Each step is equivalent to 0.125dB
SAR 5350-5470 MHz Set1 Chain B	<b>minimum = 0</b> <b>maximum = 0xFF</b> <b>step = 1</b> <b>default = 0</b>	Defines the WiFi SAR Tx Power Limit - 8bit unsigned with 5bit integer and 3bit fractional. 0x00 = 0b00000000 = 0.125dB; 0xFF = 0b11111111 = 31.875dB. Each step is equivalent to 0.125dB
SAR 5470-5725 MHz Set1 Chain B	<b>minimum = 0</b> <b>maximum = 0xFF</b> <b>step = 1</b> <b>default = 0</b>	Defines the WiFi SAR Tx Power Limit - 8bit unsigned with 5bit integer and 3bit fractional. 0x00 = 0b00000000 = 0.125dB; 0xFF = 0b11111111 = 31.875dB. Each step is equivalent to 0.125dB
SAR 5725-5925 MHz Set1 Chain B	<b>minimum = 0</b> <b>maximum = 0xFF</b> <b>step = 1</b> <b>default = 0</b>	Defines the WiFi SAR Tx Power Limit - 8bit unsigned with 5bit integer and 3bit fractional. 0x00 = 0b00000000 = 0.125dB; 0xFF = 0b11111111 = 31.875dB. Each step is equivalent to 0.125dB
SAR 5945-6165 MHz Set1 Chain B	<b>minimum = 0</b> <b>maximum = 0xFF</b> <b>step = 1</b> <b>default = 0</b>	Defines the WiFi SAR Tx Power Limit - 8bit unsigned with 5bit integer and 3bit fractional. 0x00 = 0b00000000 = 0.125dB; 0xFF = 0b11111111 = 31.875dB. Each step is equivalent to 0.125dB
SAR 6165-6405 MHz Set1 Chain B	<b>minimum = 0</b> <b>maximum = 0xFF</b> <b>step = 1</b> <b>default = 0</b>	Defines the WiFi SAR Tx Power Limit - 8bit unsigned with 5bit integer and 3bit fractional. 0x00 = 0b00000000 = 0.125dB; 0xFF = 0b11111111 = 31.875dB. Each step is equivalent to 0.125dB
SAR 6405-6525 MHz Set1 Chain B	<b>minimum = 0</b> <b>maximum = 0xFF</b> <b>step = 1</b> <b>default = 0</b>	Defines the WiFi SAR Tx Power Limit - 8bit unsigned with 5bit integer and 3bit fractional. 0x00 = 0b00000000 = 0.125dB; 0xFF = 0b11111111 = 31.875dB. Each step is equivalent to 0.125dB
SAR 6525-6705 MHz Set1 Chain B	<b>minimum = 0</b> <b>maximum = 0xFF</b> <b>step = 1</b> <b>default = 0</b>	Defines the WiFi SAR Tx Power Limit - 8bit unsigned with 5bit integer and 3bit fractional. 0x00 = 0b00000000 = 0.125dB; 0xFF = 0b11111111 = 31.875dB. Each step is equivalent to 0.125dB
SAR 6705-6865 MHz Set1 Chain B	<b>minimum = 0</b> <b>maximum = 0xFF</b> <b>step = 1</b> <b>default = 0</b>	Defines the WiFi SAR Tx Power Limit - 8bit unsigned with 5bit integer and 3bit fractional. 0x00 = 0b00000000 = 0.125dB; 0xFF = 0b11111111 =

			31.875dB. Each step is equivalent to 0.125dB
SAR 6865-7105 MHz Set1 Chain B	<b>minimum = 0</b> <b>maximum = 0xFF</b> <b>step = 1</b> <b>default = 0</b>		Defines the WiFi SAR Tx Power Limit - 8bit unsigned with 5bit integer and 3bit fractional. 0x00 = 0b00000000 = 0.125dB; 0xFF = 0b11111111 = 31.875dB. Each step is equivalent to 0.125dB
SAR CDB 2400 MHz Set1 Chain A	<b>minimum = 0</b> <b>maximum = 0xFF</b> <b>step = 1</b> <b>default = 0</b>		Defines the WiFi CDB SAR Tx Power Limit - 8bit unsigned with 5bit integer and 3bit fractional. 0x00 = 0b00000000 = 0.125dB; 0xFF = 0b11111111 = 31.875dB. Each step is equivalent to 0.125dB
SAR CDB 5150-5350 MHz Set1 Chain A	<b>minimum = 0</b> <b>maximum = 0xFF</b> <b>step = 1</b> <b>default = 0</b>		Defines the WiFi CDB SAR Tx Power Limit - 8bit unsigned with 5bit integer and 3bit fractional. 0x00 = 0b00000000 = 0.125dB; 0xFF = 0b11111111 = 31.875dB. Each step is equivalent to 0.125dB
SAR CDB 5350-5470 MHz Set1 Chain A	<b>minimum = 0</b> <b>maximum = 0xFF</b> <b>step = 1</b> <b>default = 0</b>		Defines the WiFi CDB SAR Tx Power Limit - 8bit unsigned with 5bit integer and 3bit fractional. 0x00 = 0b00000000 = 0.125dB; 0xFF = 0b11111111 = 31.875dB. Each step is equivalent to 0.125dB
SAR CDB 5470-5725 MHz Set1 Chain A	<b>minimum = 0</b> <b>maximum = 0xFF</b> <b>step = 1</b> <b>default = 0</b>		Defines the WiFi CDB SAR Tx Power Limit - 8bit unsigned with 5bit integer and 3bit fractional. 0x00 = 0b00000000 = 0.125dB; 0xFF = 0b11111111 = 31.875dB. Each step is equivalent to 0.125dB
SAR CDB 5725-5925 MHz Set1 Chain A	<b>minimum = 0</b> <b>maximum = 0xFF</b> <b>step = 1</b> <b>default = 0</b>		Defines the WiFi CDB SAR Tx Power Limit - 8bit unsigned with 5bit integer and 3bit fractional. 0x00 = 0b00000000 = 0.125dB; 0xFF = 0b11111111 = 31.875dB. Each step is equivalent to 0.125dB
SAR CDB 5945-6165 MHz Set1 Chain A	<b>minimum = 0</b> <b>maximum = 0xFF</b> <b>step = 1</b> <b>default = 0</b>		Defines the WiFi CDB SAR Tx Power Limit - 8bit unsigned with 5bit integer and 3bit fractional. 0x00 = 0b00000000 = 0.125dB; 0xFF = 0b11111111 = 31.875dB. Each step is equivalent to 0.125dB
SAR CDB 6165-6405 MHz Set1 Chain A	<b>minimum = 0</b> <b>maximum = 0xFF</b> <b>step = 1</b> <b>default = 0</b>		Defines the WiFi CDB SAR Tx Power Limit - 8bit unsigned with 5bit integer and 3bit fractional. 0x00 = 0b00000000 = 0.125dB; 0xFF = 0b11111111 = 31.875dB. Each step is equivalent to 0.125dB

SAR CDB 6405-6525 MHz Set1 Chain A	<b>minimum = 0</b> <b>maximum = 0xFF</b> <b>step = 1</b> <b>default = 0</b>	Defines the WiFi CDB SAR Tx Power Limit - 8bit unsigned with 5bit integer and 3bit fractional. 0x00 = 0b00000000 = 0.125dB; 0xFF = 0b11111111 = 31.875dB. Each step is equivalent to 0.125dB
SAR CDB 6525-6705 MHz Set1 Chain A	<b>minimum = 0</b> <b>maximum = 0xFF</b> <b>step = 1</b> <b>default = 0</b>	Defines the WiFi CDB SAR Tx Power Limit - 8bit unsigned with 5bit integer and 3bit fractional. 0x00 = 0b00000000 = 0.125dB; 0xFF = 0b11111111 = 31.875dB. Each step is equivalent to 0.125dB
SAR CDB 6705-6865 MHz Set1 Chain A	<b>minimum = 0</b> <b>maximum = 0xFF</b> <b>step = 1</b> <b>default = 0</b>	Defines the WiFi CDB SAR Tx Power Limit - 8bit unsigned with 5bit integer and 3bit fractional. 0x00 = 0b00000000 = 0.125dB; 0xFF = 0b11111111 = 31.875dB. Each step is equivalent to 0.125dB
SAR CDB 6865-7105 MHz Set1 Chain A	<b>minimum = 0</b> <b>maximum = 0xFF</b> <b>step = 1</b> <b>default = 0</b>	Defines the WiFi CDB SAR Tx Power Limit - 8bit unsigned with 5bit integer and 3bit fractional. 0x00 = 0b00000000 = 0.125dB; 0xFF = 0b11111111 = 31.875dB. Each step is equivalent to 0.125dB
SAR CDB 2400 MHz Set1 Chain B	<b>minimum = 0</b> <b>maximum = 0xFF</b> <b>step = 1</b> <b>default = 0</b>	Defines the WiFi CDB SAR Tx Power Limit - 8bit unsigned with 5bit integer and 3bit fractional. 0x00 = 0b00000000 = 0.125dB; 0xFF = 0b11111111 = 31.875dB. Each step is equivalent to 0.125dB
SAR CDB 5150-5350 MHz Set1 Chain B	<b>minimum = 0</b> <b>maximum = 0xFF</b> <b>step = 1</b> <b>default = 0</b>	Defines the WiFi CDB SAR Tx Power Limit - 8bit unsigned with 5bit integer and 3bit fractional. 0x00 = 0b00000000 = 0.125dB; 0xFF = 0b11111111 = 31.875dB. Each step is equivalent to 0.125dB
SAR CDB 5350-5470 MHz Set1 Chain B	<b>minimum = 0</b> <b>maximum = 0xFF</b> <b>step = 1</b> <b>default = 0</b>	Defines the WiFi CDB SAR Tx Power Limit - 8bit unsigned with 5bit integer and 3bit fractional. 0x00 = 0b00000000 = 0.125dB; 0xFF = 0b11111111 = 31.875dB. Each step is equivalent to 0.125dB
SAR CDB 5470-5725 MHz Set1 Chain B	<b>minimum = 0</b> <b>maximum = 0xFF</b> <b>step = 1</b> <b>default = 0</b>	Defines the WiFi CDB SAR Tx Power Limit - 8bit unsigned with 5bit integer and 3bit fractional. 0x00 = 0b00000000 = 0.125dB; 0xFF = 0b11111111 = 31.875dB. Each step is equivalent to 0.125dB
SAR CDB 5725-5925 MHz Set1 Chain B	<b>minimum = 0</b> <b>maximum = 0xFF</b> <b>step = 1</b>	Defines the WiFi CDB SAR Tx Power Limit - 8bit unsigned with 5bit integer and 3bit fractional. 0x00 =

		<b>default = 0</b>	0b00000000 = 0.125dB; 0xFF = 0b11111111 = 31.875dB. Each step is equivalent to 0.125dB
SAR CDB 5945-6165 MHz Set1 Chain B		<b>minimum = 0</b> <b>maximum = 0xFF</b> <b>step = 1</b> <b>default = 0</b>	Defines the WiFi CDB SAR Tx Power Limit - 8bit unsigned with 5bit integer and 3bit fractional. 0x00 = 0b00000000 = 0.125dB; 0xFF = 0b11111111 = 31.875dB. Each step is equivalent to 0.125dB
SAR CDB 6165-6405 MHz Set1 Chain B		<b>minimum = 0</b> <b>maximum = 0xFF</b> <b>step = 1</b> <b>default = 0</b>	Defines the WiFi CDB SAR Tx Power Limit - 8bit unsigned with 5bit integer and 3bit fractional. 0x00 = 0b00000000 = 0.125dB; 0xFF = 0b11111111 = 31.875dB. Each step is equivalent to 0.125dB
SAR CDB 6405-6525 MHz Set1 Chain B		<b>minimum = 0</b> <b>maximum = 0xFF</b> <b>step = 1</b> <b>default = 0</b>	Defines the WiFi CDB SAR Tx Power Limit - 8bit unsigned with 5bit integer and 3bit fractional. 0x00 = 0b00000000 = 0.125dB; 0xFF = 0b11111111 = 31.875dB. Each step is equivalent to 0.125dB
SAR CDB 6525-6705 MHz Set1 Chain B		<b>minimum = 0</b> <b>maximum = 0xFF</b> <b>step = 1</b> <b>default = 0</b>	Defines the WiFi CDB SAR Tx Power Limit - 8bit unsigned with 5bit integer and 3bit fractional. 0x00 = 0b00000000 = 0.125dB; 0xFF = 0b11111111 = 31.875dB. Each step is equivalent to 0.125dB
SAR CDB 6705-6865 MHz Set1 Chain B		<b>minimum = 0</b> <b>maximum = 0xFF</b> <b>step = 1</b> <b>default = 0</b>	Defines the WiFi CDB SAR Tx Power Limit - 8bit unsigned with 5bit integer and 3bit fractional. 0x00 = 0b00000000 = 0.125dB; 0xFF = 0b11111111 = 31.875dB. Each step is equivalent to 0.125dB
SAR CDB 6865-7105 MHz Set1 Chain B		<b>minimum = 0</b> <b>maximum = 0xFF</b> <b>step = 1</b> <b>default = 0</b>	Defines the WiFi CDB SAR Tx Power Limit - 8bit unsigned with 5bit integer and 3bit fractional. 0x00 = 0b00000000 = 0.125dB; 0xFF = 0b11111111 = 31.875dB. Each step is equivalent to 0.125dB
EWRD Package		No options	EWRD Package
WiFi Dynamic SAR		<b>[Disabled]</b> [Enabled]	Enable/Disable WiFi Dynamic SAR Tx Power Limit which shall be set dynamically according to the Proximity Sensor <u>(Below options will show at this option set Enabled)</u>

Extended SAR Range Sets	<b>[No Additional sets]</b> [Set 2] [Set 3] [Set 4]	Defines the WiFi SAR Sets that can be used to set the power limits dynamically based on the Proximity Sensor, Set 1 is always present if WiFi SAR is enabled and Set 2-3 are additional sets
SAR 2400 MHz Set2 Chain A	<b>minimum = 0</b> <b>maximum = 0xFF</b> <b>step = 1</b> <b>default = 0</b>	Defines the WiFi SAR Tx Power Limit - 8bit unsigned with 5bit integer and 3bit fractional. 0x00 = 0b00000000 = 0.125dB; 0xFF = 0b11111111 = 31.875dB. Each step is equivalent to 0.125dB
SAR 5150-5350 MHz Set2 Chain A	<b>minimum = 0</b> <b>maximum = 0xFF</b> <b>step = 1</b> <b>default = 0</b>	Defines the WiFi SAR Tx Power Limit - 8bit unsigned with 5bit integer and 3bit fractional. 0x00 = 0b00000000 = 0.125dB; 0xFF = 0b11111111 = 31.875dB. Each step is equivalent to 0.125dB
SAR 5350-5470 MHz Set2 Chain A	<b>minimum = 0</b> <b>maximum = 0xFF</b> <b>step = 1</b> <b>default = 0</b>	Defines the WiFi SAR Tx Power Limit - 8bit unsigned with 5bit integer and 3bit fractional. 0x00 = 0b00000000 = 0.125dB; 0xFF = 0b11111111 = 31.875dB. Each step is equivalent to 0.125dB
SAR 5470-5725 MHz Set2 Chain A	<b>minimum = 0</b> <b>maximum = 0xFF</b> <b>step = 1</b> <b>default = 0</b>	Defines the WiFi SAR Tx Power Limit - 8bit unsigned with 5bit integer and 3bit fractional. 0x00 = 0b00000000 = 0.125dB; 0xFF = 0b11111111 = 31.875dB. Each step is equivalent to 0.125dB
SAR 5725-5925 MHz Set2 Chain A	<b>minimum = 0</b> <b>maximum = 0xFF</b> <b>step = 1</b> <b>default = 0</b>	Defines the WiFi SAR Tx Power Limit - 8bit unsigned with 5bit integer and 3bit fractional. 0x00 = 0b00000000 = 0.125dB; 0xFF = 0b11111111 = 31.875dB. Each step is equivalent to 0.125dB
SAR 5945-6165 MHz Set2 Chain A	<b>minimum = 0</b> <b>maximum = 0xFF</b> <b>step = 1</b> <b>default = 0</b>	Defines the WiFi SAR Tx Power Limit - 8bit unsigned with 5bit integer and 3bit fractional. 0x00 = 0b00000000 = 0.125dB; 0xFF = 0b11111111 = 31.875dB. Each step is equivalent to 0.125dB
SAR 6165-6405 MHz Set2 Chain A	<b>minimum = 0</b> <b>maximum = 0xFF</b> <b>step = 1</b> <b>default = 0</b>	Defines the WiFi SAR Tx Power Limit - 8bit unsigned with 5bit integer and 3bit fractional. 0x00 = 0b00000000 = 0.125dB; 0xFF = 0b11111111 = 31.875dB. Each step is equivalent to 0.125dB

SAR 6405-6525 MHz Set2 Chain A	<b>minimum = 0</b> <b>maximum = 0xFF</b> <b>step = 1</b> <b>default = 0</b>	Defines the WiFi SAR Tx Power Limit - 8bit unsigned with 5bit integer and 3bit fractional. 0x00 = 0b00000000 = 0.125dB; 0xFF = 0b11111111 = 31.875dB. Each step is equivalent to 0.125dB
SAR 6525-6705 MHz Set2 Chain A	<b>minimum = 0</b> <b>maximum = 0xFF</b> <b>step = 1</b> <b>default = 0</b>	Defines the WiFi SAR Tx Power Limit - 8bit unsigned with 5bit integer and 3bit fractional. 0x00 = 0b00000000 = 0.125dB; 0xFF = 0b11111111 = 31.875dB. Each step is equivalent to 0.125dB
SAR 6705-6865 MHz Set2 Chain A	<b>minimum = 0</b> <b>maximum = 0xFF</b> <b>step = 1</b> <b>default = 0</b>	Defines the WiFi SAR Tx Power Limit - 8bit unsigned with 5bit integer and 3bit fractional. 0x00 = 0b00000000 = 0.125dB; 0xFF = 0b11111111 = 31.875dB. Each step is equivalent to 0.125dB
SAR 6865-7105 MHz Set2 Chain A	<b>minimum = 0</b> <b>maximum = 0xFF</b> <b>step = 1</b> <b>default = 0</b>	Defines the WiFi SAR Tx Power Limit - 8bit unsigned with 5bit integer and 3bit fractional. 0x00 = 0b00000000 = 0.125dB; 0xFF = 0b11111111 = 31.875dB. Each step is equivalent to 0.125dB
SAR 2400 MHz Set2 Chain B	<b>minimum = 0</b> <b>maximum = 0xFF</b> <b>step = 1</b> <b>default = 0</b>	Defines the WiFi SAR Tx Power Limit - 8bit unsigned with 5bit integer and 3bit fractional. 0x00 = 0b00000000 = 0.125dB; 0xFF = 0b11111111 = 31.875dB. Each step is equivalent to 0.125dB
SAR 5150-5350 MHz Set2 Chain B	<b>minimum = 0</b> <b>maximum = 0xFF</b> <b>step = 1</b> <b>default = 0</b>	Defines the WiFi SAR Tx Power Limit - 8bit unsigned with 5bit integer and 3bit fractional. 0x00 = 0b00000000 = 0.125dB; 0xFF = 0b11111111 = 31.875dB. Each step is equivalent to 0.125dB
SAR 5350-5470 MHz Set2 Chain B	<b>minimum = 0</b> <b>maximum = 0xFF</b> <b>step = 1</b> <b>default = 0</b>	Defines the WiFi SAR Tx Power Limit - 8bit unsigned with 5bit integer and 3bit fractional. 0x00 = 0b00000000 = 0.125dB; 0xFF = 0b11111111 = 31.875dB. Each step is equivalent to 0.125dB
SAR 5470-5725 MHz Set2 Chain B	<b>minimum = 0</b> <b>maximum = 0xFF</b> <b>step = 1</b> <b>default = 0</b>	Defines the WiFi SAR Tx Power Limit - 8bit unsigned with 5bit integer and 3bit fractional. 0x00 = 0b00000000 = 0.125dB; 0xFF = 0b11111111 = 31.875dB. Each step is equivalent to 0.125dB
SAR 5725-5925 MHz Set2 Chain B	<b>minimum = 0</b> <b>maximum = 0xFF</b> <b>step = 1</b>	Defines the WiFi SAR Tx Power Limit - 8bit unsigned with 5bit integer and 3bit fractional. 0x00 = 0b00000000 =

	<b>default = 0</b>	0.125dB; 0xFF = 0b11111111 = 31.875dB. Each step is equivalent to 0.125dB
SAR 5945-6165 MHz Set2 Chain B	<b>minimum = 0</b> <b>maximum = 0xFF</b> <b>step = 1</b> <b>default = 0</b>	Defines the WiFi SAR Tx Power Limit - 8bit unsigned with 5bit integer and 3bit fractional. 0x00 = 0b00000000 = 0.125dB; 0xFF = 0b11111111 = 31.875dB. Each step is equivalent to 0.125dB
SAR 6165-6405 MHz Set2 Chain B	<b>minimum = 0</b> <b>maximum = 0xFF</b> <b>step = 1</b> <b>default = 0</b>	Defines the WiFi SAR Tx Power Limit - 8bit unsigned with 5bit integer and 3bit fractional. 0x00 = 0b00000000 = 0.125dB; 0xFF = 0b11111111 = 31.875dB. Each step is equivalent to 0.125dB
SAR 6405-6525 MHz Set2 Chain B	<b>minimum = 0</b> <b>maximum = 0xFF</b> <b>step = 1</b> <b>default = 0</b>	Defines the WiFi SAR Tx Power Limit - 8bit unsigned with 5bit integer and 3bit fractional. 0x00 = 0b00000000 = 0.125dB; 0xFF = 0b11111111 = 31.875dB. Each step is equivalent to 0.125dB
SAR 6525-6705 MHz Set2 Chain B	<b>minimum = 0</b> <b>maximum = 0xFF</b> <b>step = 1</b> <b>default = 0</b>	Defines the WiFi SAR Tx Power Limit - 8bit unsigned with 5bit integer and 3bit fractional. 0x00 = 0b00000000 = 0.125dB; 0xFF = 0b11111111 = 31.875dB. Each step is equivalent to 0.125dB
SAR 6705-6865 MHz Set2 Chain B	<b>minimum = 0</b> <b>maximum = 0xFF</b> <b>step = 1</b> <b>default = 0</b>	Defines the WiFi SAR Tx Power Limit - 8bit unsigned with 5bit integer and 3bit fractional. 0x00 = 0b00000000 = 0.125dB; 0xFF = 0b11111111 = 31.875dB. Each step is equivalent to 0.125dB
SAR 6865-7105 MHz Set2 Chain B	<b>minimum = 0</b> <b>maximum = 0xFF</b> <b>step = 1</b> <b>default = 0</b>	Defines the WiFi SAR Tx Power Limit - 8bit unsigned with 5bit integer and 3bit fractional. 0x00 = 0b00000000 = 0.125dB; 0xFF = 0b11111111 = 31.875dB. Each step is equivalent to 0.125dB
SAR 2400 MHz Set3 Chain A	<b>minimum = 0</b> <b>maximum = 0xFF</b> <b>step = 1</b> <b>default = 0</b>	Defines the WiFi SAR Tx Power Limit - 8bit unsigned with 5bit integer and 3bit fractional. 0x00 = 0b00000000 = 0.125dB; 0xFF = 0b11111111 = 31.875dB. Each step is equivalent to 0.125dB
SAR 5150-5350 MHz Set3 Chain A	<b>minimum = 0</b> <b>maximum = 0xFF</b> <b>step = 1</b> <b>default = 0</b>	Defines the WiFi SAR Tx Power Limit - 8bit unsigned with 5bit integer and 3bit fractional. 0x00 = 0b00000000 = 0.125dB; 0xFF = 0b11111111 = 31.875dB. Each step is equivalent to 0.125dB

SAR 5350-5470 MHz Set3 Chain A	<b>minimum = 0</b> <b>maximum = 0xFF</b> <b>step = 1</b> <b>default = 0</b>	Defines the WiFi SAR Tx Power Limit - 8bit unsigned with 5bit integer and 3bit fractional. 0x00 = 0b00000000 = 0.125dB; 0xFF = 0b11111111 = 31.875dB. Each step is equivalent to 0.125dB
SAR 5470-5725 MHz Set3 Chain A	<b>minimum = 0</b> <b>maximum = 0xFF</b> <b>step = 1</b> <b>default = 0</b>	Defines the WiFi SAR Tx Power Limit - 8bit unsigned with 5bit integer and 3bit fractional. 0x00 = 0b00000000 = 0.125dB; 0xFF = 0b11111111 = 31.875dB. Each step is equivalent to 0.125dB
SAR 5725-5925 MHz Set3 Chain A	<b>minimum = 0</b> <b>maximum = 0xFF</b> <b>step = 1</b> <b>default = 0</b>	Defines the WiFi SAR Tx Power Limit - 8bit unsigned with 5bit integer and 3bit fractional. 0x00 = 0b00000000 = 0.125dB; 0xFF = 0b11111111 = 31.875dB. Each step is equivalent to 0.125dB
SAR 5945-6165 MHz Set3 Chain A	<b>minimum = 0</b> <b>maximum = 0xFF</b> <b>step = 1</b> <b>default = 0</b>	Defines the WiFi SAR Tx Power Limit - 8bit unsigned with 5bit integer and 3bit fractional. 0x00 = 0b00000000 = 0.125dB; 0xFF = 0b11111111 = 31.875dB. Each step is equivalent to 0.125dB
SAR 6165-6405 MHz Set3 Chain A	<b>minimum = 0</b> <b>maximum = 0xFF</b> <b>step = 1</b> <b>default = 0</b>	Defines the WiFi SAR Tx Power Limit - 8bit unsigned with 5bit integer and 3bit fractional. 0x00 = 0b00000000 = 0.125dB; 0xFF = 0b11111111 = 31.875dB. Each step is equivalent to 0.125dB
SAR 6405-6525 MHz Set3 Chain A	<b>minimum = 0</b> <b>maximum = 0xFF</b> <b>step = 1</b> <b>default = 0</b>	Defines the WiFi SAR Tx Power Limit - 8bit unsigned with 5bit integer and 3bit fractional. 0x00 = 0b00000000 = 0.125dB; 0xFF = 0b11111111 = 31.875dB. Each step is equivalent to 0.125dB
SAR 6525-6705 MHz Set3 Chain A	<b>minimum = 0</b> <b>maximum = 0xFF</b> <b>step = 1</b> <b>default = 0</b>	Defines the WiFi SAR Tx Power Limit - 8bit unsigned with 5bit integer and 3bit fractional. 0x00 = 0b00000000 = 0.125dB; 0xFF = 0b11111111 = 31.875dB. Each step is equivalent to 0.125dB
SAR 6705-6865 MHz Set3 Chain A	<b>minimum = 0</b> <b>maximum = 0xFF</b> <b>step = 1</b> <b>default = 0</b>	Defines the WiFi SAR Tx Power Limit - 8bit unsigned with 5bit integer and 3bit fractional. 0x00 = 0b00000000 = 0.125dB; 0xFF = 0b11111111 = 31.875dB. Each step is equivalent to 0.125dB
SAR 6865-7105 MHz Set3 Chain A	<b>minimum = 0</b> <b>maximum = 0xFF</b> <b>step = 1</b>	Defines the WiFi SAR Tx Power Limit - 8bit unsigned with 5bit integer and 3bit fractional. 0x00 = 0b00000000 =

	<b>default = 0</b>	0.125dB; 0xFF = 0b11111111 = 31.875dB. Each step is equivalent to 0.125dB
SAR 2400 MHz Set3 Chain B	<b>minimum = 0</b> <b>maximum = 0xFF</b> <b>step = 1</b> <b>default = 0</b>	Defines the WiFi SAR Tx Power Limit - 8bit unsigned with 5bit integer and 3bit fractional. 0x00 = 0b00000000 = 0.125dB; 0xFF = 0b11111111 = 31.875dB. Each step is equivalent to 0.125dB
SAR 5150-5350 MHz Set3 Chain B	<b>minimum = 0</b> <b>maximum = 0xFF</b> <b>step = 1</b> <b>default = 0</b>	Defines the WiFi SAR Tx Power Limit - 8bit unsigned with 5bit integer and 3bit fractional. 0x00 = 0b00000000 = 0.125dB; 0xFF = 0b11111111 = 31.875dB. Each step is equivalent to 0.125dB
SAR 5350-5470 MHz Set3 Chain B	<b>minimum = 0</b> <b>maximum = 0xFF</b> <b>step = 1</b> <b>default = 0</b>	Defines the WiFi SAR Tx Power Limit - 8bit unsigned with 5bit integer and 3bit fractional. 0x00 = 0b00000000 = 0.125dB; 0xFF = 0b11111111 = 31.875dB. Each step is equivalent to 0.125dB
SAR 5470-5725 MHz Set3 Chain B	<b>minimum = 0</b> <b>maximum = 0xFF</b> <b>step = 1</b> <b>default = 0</b>	Defines the WiFi SAR Tx Power Limit - 8bit unsigned with 5bit integer and 3bit fractional. 0x00 = 0b00000000 = 0.125dB; 0xFF = 0b11111111 = 31.875dB. Each step is equivalent to 0.125dB
SAR 5725-5925 MHz Set3 Chain B	<b>minimum = 0</b> <b>maximum = 0xFF</b> <b>step = 1</b> <b>default = 0</b>	Defines the WiFi SAR Tx Power Limit - 8bit unsigned with 5bit integer and 3bit fractional. 0x00 = 0b00000000 = 0.125dB; 0xFF = 0b11111111 = 31.875dB. Each step is equivalent to 0.125dB
SAR 5945-6165 MHz Set3 Chain B	<b>minimum = 0</b> <b>maximum = 0xFF</b> <b>step = 1</b> <b>default = 0</b>	Defines the WiFi SAR Tx Power Limit - 8bit unsigned with 5bit integer and 3bit fractional. 0x00 = 0b00000000 = 0.125dB; 0xFF = 0b11111111 = 31.875dB. Each step is equivalent to 0.125dB
SAR 6165-6405 MHz Set3 Chain B	<b>minimum = 0</b> <b>maximum = 0xFF</b> <b>step = 1</b> <b>default = 0</b>	Defines the WiFi SAR Tx Power Limit - 8bit unsigned with 5bit integer and 3bit fractional. 0x00 = 0b00000000 = 0.125dB; 0xFF = 0b11111111 = 31.875dB. Each step is equivalent to 0.125dB
SAR 6405-6525 MHz Set3 Chain B	<b>minimum = 0</b> <b>maximum = 0xFF</b> <b>step = 1</b> <b>default = 0</b>	Defines the WiFi SAR Tx Power Limit - 8bit unsigned with 5bit integer and 3bit fractional. 0x00 = 0b00000000 = 0.125dB; 0xFF = 0b11111111 = 31.875dB. Each step is equivalent to 0.125dB

SAR 6525-6705 MHz Set3 Chain B	<b>minimum = 0</b> <b>maximum = 0xFF</b> <b>step = 1</b> <b>default = 0</b>	Defines the WiFi SAR Tx Power Limit - 8bit unsigned with 5bit integer and 3bit fractional. 0x00 = 0b00000000 = 0.125dB; 0xFF = 0b11111111 = 31.875dB. Each step is equivalent to 0.125dB
SAR 6705-6865 MHz Set3 Chain B	<b>minimum = 0</b> <b>maximum = 0xFF</b> <b>step = 1</b> <b>default = 0</b>	Defines the WiFi SAR Tx Power Limit - 8bit unsigned with 5bit integer and 3bit fractional. 0x00 = 0b00000000 = 0.125dB; 0xFF = 0b11111111 = 31.875dB. Each step is equivalent to 0.125dB
SAR 6865-7105 MHz Set3 Chain B	<b>minimum = 0</b> <b>maximum = 0xFF</b> <b>step = 1</b> <b>default = 0</b>	Defines the WiFi SAR Tx Power Limit - 8bit unsigned with 5bit integer and 3bit fractional. 0x00 = 0b00000000 = 0.125dB; 0xFF = 0b11111111 = 31.875dB. Each step is equivalent to 0.125dB
SAR 2400 MHz Set4 Chain A	<b>minimum = 0</b> <b>maximum = 0xFF</b> <b>step = 1</b> <b>default = 0</b>	Defines the WiFi SAR Tx Power Limit - 8bit unsigned with 5bit integer and 3bit fractional. 0x00 = 0b00000000 = 0.125dB; 0xFF = 0b11111111 = 31.875dB. Each step is equivalent to 0.125dB
SAR 5150-5350 MHz Set4 Chain A	<b>minimum = 0</b> <b>maximum = 0xFF</b> <b>step = 1</b> <b>default = 0</b>	Defines the WiFi SAR Tx Power Limit - 8bit unsigned with 5bit integer and 3bit fractional. 0x00 = 0b00000000 = 0.125dB; 0xFF = 0b11111111 = 31.875dB. Each step is equivalent to 0.125dB
SAR 5350-5470 MHz Set4 Chain A	<b>minimum = 0</b> <b>maximum = 0xFF</b> <b>step = 1</b> <b>default = 0</b>	Defines the WiFi SAR Tx Power Limit - 8bit unsigned with 5bit integer and 3bit fractional. 0x00 = 0b00000000 = 0.125dB; 0xFF = 0b11111111 = 31.875dB. Each step is equivalent to 0.125dB
SAR 5470-5725 MHz Set4 Chain A	<b>minimum = 0</b> <b>maximum = 0xFF</b> <b>step = 1</b> <b>default = 0</b>	Defines the WiFi SAR Tx Power Limit - 8bit unsigned with 5bit integer and 3bit fractional. 0x00 = 0b00000000 = 0.125dB; 0xFF = 0b11111111 = 31.875dB. Each step is equivalent to 0.125dB
SAR 5725-5925 MHz Set4 Chain A	<b>minimum = 0</b> <b>maximum = 0xFF</b> <b>step = 1</b> <b>default = 0</b>	Defines the WiFi SAR Tx Power Limit - 8bit unsigned with 5bit integer and 3bit fractional. 0x00 = 0b00000000 = 0.125dB; 0xFF = 0b11111111 = 31.875dB. Each step is equivalent to 0.125dB
SAR 5945-6165 MHz Set4 Chain A	<b>minimum = 0</b> <b>maximum = 0xFF</b> <b>step = 1</b>	Defines the WiFi SAR Tx Power Limit - 8bit unsigned with 5bit integer and 3bit fractional. 0x00 = 0b00000000 =

		<b>default = 0</b>	0.125dB; 0xFF = 0b11111111 = 31.875dB. Each step is equivalent to 0.125dB
SAR 6165-6405 MHz Set4 Chain A		<b>minimum = 0</b> <b>maximum = 0xFF</b> <b>step = 1</b> <b>default = 0</b>	Defines the WiFi SAR Tx Power Limit - 8bit unsigned with 5bit integer and 3bit fractional. 0x00 = 0b00000000 = 0.125dB; 0xFF = 0b11111111 = 31.875dB. Each step is equivalent to 0.125dB
SAR 6405-6525 MHz Set4 Chain A		<b>minimum = 0</b> <b>maximum = 0xFF</b> <b>step = 1</b> <b>default = 0</b>	Defines the WiFi SAR Tx Power Limit - 8bit unsigned with 5bit integer and 3bit fractional. 0x00 = 0b00000000 = 0.125dB; 0xFF = 0b11111111 = 31.875dB. Each step is equivalent to 0.125dB
SAR 6525-6705 MHz Set4 Chain A		<b>minimum = 0</b> <b>maximum = 0xFF</b> <b>step = 1</b> <b>default = 0</b>	Defines the WiFi SAR Tx Power Limit - 8bit unsigned with 5bit integer and 3bit fractional. 0x00 = 0b00000000 = 0.125dB; 0xFF = 0b11111111 = 31.875dB. Each step is equivalent to 0.125dB
SAR 6705-6865 MHz Set4 Chain A		<b>minimum = 0</b> <b>maximum = 0xFF</b> <b>step = 1</b> <b>default = 0</b>	Defines the WiFi SAR Tx Power Limit - 8bit unsigned with 5bit integer and 3bit fractional. 0x00 = 0b00000000 = 0.125dB; 0xFF = 0b11111111 = 31.875dB. Each step is equivalent to 0.125dB
SAR 6865-7105 MHz Set4 Chain A		<b>minimum = 0</b> <b>maximum = 0xFF</b> <b>step = 1</b> <b>default = 0</b>	Defines the WiFi SAR Tx Power Limit - 8bit unsigned with 5bit integer and 3bit fractional. 0x00 = 0b00000000 = 0.125dB; 0xFF = 0b11111111 = 31.875dB. Each step is equivalent to 0.125dB
SAR 2400 MHz Set4 Chain B		<b>minimum = 0</b> <b>maximum = 0xFF</b> <b>step = 1</b> <b>default = 0</b>	Defines the WiFi SAR Tx Power Limit - 8bit unsigned with 5bit integer and 3bit fractional. 0x00 = 0b00000000 = 0.125dB; 0xFF = 0b11111111 = 31.875dB. Each step is equivalent to 0.125dB
SAR 5150-5350 MHz Set4 Chain B		<b>minimum = 0</b> <b>maximum = 0xFF</b> <b>step = 1</b> <b>default = 0</b>	Defines the WiFi SAR Tx Power Limit - 8bit unsigned with 5bit integer and 3bit fractional. 0x00 = 0b00000000 = 0.125dB; 0xFF = 0b11111111 = 31.875dB. Each step is equivalent to 0.125dB
SAR 5350-5470 MHz Set4 Chain B		<b>minimum = 0</b> <b>maximum = 0xFF</b> <b>step = 1</b> <b>default = 0</b>	Defines the WiFi SAR Tx Power Limit - 8bit unsigned with 5bit integer and 3bit fractional. 0x00 = 0b00000000 = 0.125dB; 0xFF = 0b11111111 = 31.875dB. Each step is equivalent to 0.125dB

SAR 5470-5725 MHz Set4 Chain B	<b>minimum = 0</b> <b>maximum = 0xFF</b> <b>step = 1</b> <b>default = 0</b>	Defines the WiFi SAR Tx Power Limit - 8bit unsigned with 5bit integer and 3bit fractional. 0x00 = 0b00000000 = 0.125dB; 0xFF = 0b11111111 = 31.875dB. Each step is equivalent to 0.125dB
SAR 5725-5925 MHz Set4 Chain B	<b>minimum = 0</b> <b>maximum = 0xFF</b> <b>step = 1</b> <b>default = 0</b>	Defines the WiFi SAR Tx Power Limit - 8bit unsigned with 5bit integer and 3bit fractional. 0x00 = 0b00000000 = 0.125dB; 0xFF = 0b11111111 = 31.875dB. Each step is equivalent to 0.125dB
SAR 5945-6165 MHz Set4 Chain B	<b>minimum = 0</b> <b>maximum = 0xFF</b> <b>step = 1</b> <b>default = 0</b>	Defines the WiFi SAR Tx Power Limit - 8bit unsigned with 5bit integer and 3bit fractional. 0x00 = 0b00000000 = 0.125dB; 0xFF = 0b11111111 = 31.875dB. Each step is equivalent to 0.125dB
SAR 6165-6405 MHz Set4 Chain B	<b>minimum = 0</b> <b>maximum = 0xFF</b> <b>step = 1</b> <b>default = 0</b>	Defines the WiFi SAR Tx Power Limit - 8bit unsigned with 5bit integer and 3bit fractional. 0x00 = 0b00000000 = 0.125dB; 0xFF = 0b11111111 = 31.875dB. Each step is equivalent to 0.125dB
SAR 6405-6525 MHz Set4 Chain B	<b>minimum = 0</b> <b>maximum = 0xFF</b> <b>step = 1</b> <b>default = 0</b>	Defines the WiFi SAR Tx Power Limit - 8bit unsigned with 5bit integer and 3bit fractional. 0x00 = 0b00000000 = 0.125dB; 0xFF = 0b11111111 = 31.875dB. Each step is equivalent to 0.125dB
SAR 6525-6705 MHz Set4 Chain B	<b>minimum = 0</b> <b>maximum = 0xFF</b> <b>step = 1</b> <b>default = 0</b>	Defines the WiFi SAR Tx Power Limit - 8bit unsigned with 5bit integer and 3bit fractional. 0x00 = 0b00000000 = 0.125dB; 0xFF = 0b11111111 = 31.875dB. Each step is equivalent to 0.125dB
SAR 6705-6865 MHz Set4 Chain B	<b>minimum = 0</b> <b>maximum = 0xFF</b> <b>step = 1</b> <b>default = 0</b>	Defines the WiFi SAR Tx Power Limit - 8bit unsigned with 5bit integer and 3bit fractional. 0x00 = 0b00000000 = 0.125dB; 0xFF = 0b11111111 = 31.875dB. Each step is equivalent to 0.125dB
SAR 6865-7105 MHz Set4 Chain B	<b>minimum = 0</b> <b>maximum = 0xFF</b> <b>step = 1</b> <b>default = 0</b>	Defines the WiFi SAR Tx Power Limit - 8bit unsigned with 5bit integer and 3bit fractional. 0x00 = 0b00000000 = 0.125dB; 0xFF = 0b11111111 = 31.875dB. Each step is equivalent to 0.125dB
SAR CDB 2400 MHz Set2 Chain A	<b>minimum = 0</b> <b>maximum = 0xFF</b> <b>step = 1</b>	Defines the WiFi CDB SAR Tx Power Limit - 8bit unsigned with 5bit integer and 3bit fractional. 0x00 =

	<b>default = 0</b>	0b00000000 = 0.125dB; 0xFF = 0b11111111 = 31.875dB. Each step is equivalent to 0.125dB
SAR CDB 5150-5350 MHz Set2 Chain A	<b>minimum = 0</b> <b>maximum = 0xFF</b> <b>step = 1</b> <b>default = 0</b>	Defines the WiFi CDB SAR Tx Power Limit - 8bit unsigned with 5bit integer and 3bit fractional. 0x00 = 0b00000000 = 0.125dB; 0xFF = 0b11111111 = 31.875dB. Each step is equivalent to 0.125dB
SAR CDB 5350-5470 MHz Set2 Chain A	<b>minimum = 0</b> <b>maximum = 0xFF</b> <b>step = 1</b> <b>default = 0</b>	Defines the WiFi CDB SAR Tx Power Limit - 8bit unsigned with 5bit integer and 3bit fractional. 0x00 = 0b00000000 = 0.125dB; 0xFF = 0b11111111 = 31.875dB. Each step is equivalent to 0.125dB
SAR CDB 5470-5725 MHz Set2 Chain A	<b>minimum = 0</b> <b>maximum = 0xFF</b> <b>step = 1</b> <b>default = 0</b>	Defines the WiFi CDB SAR Tx Power Limit - 8bit unsigned with 5bit integer and 3bit fractional. 0x00 = 0b00000000 = 0.125dB; 0xFF = 0b11111111 = 31.875dB. Each step is equivalent to 0.125dB
SAR CDB 5725-5925 MHz Set2 Chain A	<b>minimum = 0</b> <b>maximum = 0xFF</b> <b>step = 1</b> <b>default = 0</b>	Defines the WiFi CDB SAR Tx Power Limit - 8bit unsigned with 5bit integer and 3bit fractional. 0x00 = 0b00000000 = 0.125dB; 0xFF = 0b11111111 = 31.875dB. Each step is equivalent to 0.125dB
SAR CDB 5945-6165 MHz Set2 Chain A	<b>minimum = 0</b> <b>maximum = 0xFF</b> <b>step = 1</b> <b>default = 0</b>	Defines the WiFi CDB SAR Tx Power Limit - 8bit unsigned with 5bit integer and 3bit fractional. 0x00 = 0b00000000 = 0.125dB; 0xFF = 0b11111111 = 31.875dB. Each step is equivalent to 0.125dB
SAR CDB 6165-6405 MHz Set2 Chain A	<b>minimum = 0</b> <b>maximum = 0xFF</b> <b>step = 1</b> <b>default = 0</b>	Defines the WiFi CDB SAR Tx Power Limit - 8bit unsigned with 5bit integer and 3bit fractional. 0x00 = 0b00000000 = 0.125dB; 0xFF = 0b11111111 = 31.875dB. Each step is equivalent to 0.125dB
SAR CDB 6405-6525 MHz Set2 Chain A	<b>minimum = 0</b> <b>maximum = 0xFF</b> <b>step = 1</b> <b>default = 0</b>	Defines the WiFi CDB SAR Tx Power Limit - 8bit unsigned with 5bit integer and 3bit fractional. 0x00 = 0b00000000 = 0.125dB; 0xFF = 0b11111111 = 31.875dB. Each step is equivalent to 0.125dB
SAR CDB 6525-6705 MHz Set2 Chain A	<b>minimum = 0</b> <b>maximum = 0xFF</b> <b>step = 1</b> <b>default = 0</b>	Defines the WiFi CDB SAR Tx Power Limit - 8bit unsigned with 5bit integer and 3bit fractional. 0x00 = 0b00000000 = 0.125dB; 0xFF = 0b11111111 = 31.875dB. Each step is equivalent to 0.125dB

SAR CDB 6705-6865 MHz Set2 Chain A	<b>minimum = 0</b> <b>maximum = 0xFF</b> <b>step = 1</b> <b>default = 0</b>	Defines the WiFi CDB SAR Tx Power Limit - 8bit unsigned with 5bit integer and 3bit fractional. 0x00 = 0b00000000 = 0.125dB; 0xFF = 0b11111111 = 31.875dB. Each step is equivalent to 0.125dB
SAR CDB 6865-7105 MHz Set2 Chain A	<b>minimum = 0</b> <b>maximum = 0xFF</b> <b>step = 1</b> <b>default = 0</b>	Defines the WiFi CDB SAR Tx Power Limit - 8bit unsigned with 5bit integer and 3bit fractional. 0x00 = 0b00000000 = 0.125dB; 0xFF = 0b11111111 = 31.875dB. Each step is equivalent to 0.125dB
SAR CDB 2400 MHz Set2 Chain B	<b>minimum = 0</b> <b>maximum = 0xFF</b> <b>step = 1</b> <b>default = 0</b>	Defines the WiFi CDB SAR Tx Power Limit - 8bit unsigned with 5bit integer and 3bit fractional. 0x00 = 0b00000000 = 0.125dB; 0xFF = 0b11111111 = 31.875dB. Each step is equivalent to 0.125dB
SAR CDB 5150-5350 MHz Set2 Chain B	<b>minimum = 0</b> <b>maximum = 0xFF</b> <b>step = 1</b> <b>default = 0</b>	Defines the WiFi CDB SAR Tx Power Limit - 8bit unsigned with 5bit integer and 3bit fractional. 0x00 = 0b00000000 = 0.125dB; 0xFF = 0b11111111 = 31.875dB. Each step is equivalent to 0.125dB
SAR CDB 5350-5470 MHz Set2 Chain B	<b>minimum = 0</b> <b>maximum = 0xFF</b> <b>step = 1</b> <b>default = 0</b>	Defines the WiFi CDB SAR Tx Power Limit - 8bit unsigned with 5bit integer and 3bit fractional. 0x00 = 0b00000000 = 0.125dB; 0xFF = 0b11111111 = 31.875dB. Each step is equivalent to 0.125dB
SAR CDB 5470-5725 MHz Set2 Chain B	<b>minimum = 0</b> <b>maximum = 0xFF</b> <b>step = 1</b> <b>default = 0</b>	Defines the WiFi CDB SAR Tx Power Limit - 8bit unsigned with 5bit integer and 3bit fractional. 0x00 = 0b00000000 = 0.125dB; 0xFF = 0b11111111 = 31.875dB. Each step is equivalent to 0.125dB
SAR CDB 5725-5925 MHz Set2 Chain B	<b>minimum = 0</b> <b>maximum = 0xFF</b> <b>step = 1</b> <b>default = 0</b>	Defines the WiFi CDB SAR Tx Power Limit - 8bit unsigned with 5bit integer and 3bit fractional. 0x00 = 0b00000000 = 0.125dB; 0xFF = 0b11111111 = 31.875dB. Each step is equivalent to 0.125dB
SAR CDB 5945-6165 MHz Set2 Chain B	<b>minimum = 0</b> <b>maximum = 0xFF</b> <b>step = 1</b> <b>default = 0</b>	Defines the WiFi CDB SAR Tx Power Limit - 8bit unsigned with 5bit integer and 3bit fractional. 0x00 = 0b00000000 = 0.125dB; 0xFF = 0b11111111 = 31.875dB. Each step is equivalent to 0.125dB
SAR CDB 6165-6405 MHz Set2 Chain B	<b>minimum = 0</b> <b>maximum = 0xFF</b> <b>step = 1</b>	Defines the WiFi CDB SAR Tx Power Limit - 8bit unsigned with 5bit integer and 3bit fractional. 0x00 =

		<b>default = 0</b>	0b00000000 = 0.125dB; 0xFF = 0b11111111 = 31.875dB. Each step is equivalent to 0.125dB
SAR CDB 6405-6525 MHz Set2 Chain B		<b>minimum = 0</b> <b>maximum = 0xFF</b> <b>step = 1</b> <b>default = 0</b>	Defines the WiFi CDB SAR Tx Power Limit - 8bit unsigned with 5bit integer and 3bit fractional. 0x00 = 0b00000000 = 0.125dB; 0xFF = 0b11111111 = 31.875dB. Each step is equivalent to 0.125dB
SAR CDB 6525-6705 MHz Set2 Chain B		<b>minimum = 0</b> <b>maximum = 0xFF</b> <b>step = 1</b> <b>default = 0</b>	Defines the WiFi CDB SAR Tx Power Limit - 8bit unsigned with 5bit integer and 3bit fractional. 0x00 = 0b00000000 = 0.125dB; 0xFF = 0b11111111 = 31.875dB. Each step is equivalent to 0.125dB
SAR CDB 6705-6865 MHz Set2 Chain B		<b>minimum = 0</b> <b>maximum = 0xFF</b> <b>step = 1</b> <b>default = 0</b>	Defines the WiFi CDB SAR Tx Power Limit - 8bit unsigned with 5bit integer and 3bit fractional. 0x00 = 0b00000000 = 0.125dB; 0xFF = 0b11111111 = 31.875dB. Each step is equivalent to 0.125dB
SAR CDB 6865-7105 MHz Set2 Chain B		<b>minimum = 0</b> <b>maximum = 0xFF</b> <b>step = 1</b> <b>default = 0</b>	Defines the WiFi CDB SAR Tx Power Limit - 8bit unsigned with 5bit integer and 3bit fractional. 0x00 = 0b00000000 = 0.125dB; 0xFF = 0b11111111 = 31.875dB. Each step is equivalent to 0.125dB
SAR CDB 2400 MHz Set3 Chain A		<b>minimum = 0</b> <b>maximum = 0xFF</b> <b>step = 1</b> <b>default = 0</b>	Defines the WiFi CDB SAR Tx Power Limit - 8bit unsigned with 5bit integer and 3bit fractional. 0x00 = 0b00000000 = 0.125dB; 0xFF = 0b11111111 = 31.875dB. Each step is equivalent to 0.125dB
SAR CDB 5150-5350 MHz Set3 Chain A		<b>minimum = 0</b> <b>maximum = 0xFF</b> <b>step = 1</b> <b>default = 0</b>	Defines the WiFi CDB SAR Tx Power Limit - 8bit unsigned with 5bit integer and 3bit fractional. 0x00 = 0b00000000 = 0.125dB; 0xFF = 0b11111111 = 31.875dB. Each step is equivalent to 0.125dB
SAR CDB 5350-5470 MHz Set3 Chain A		<b>minimum = 0</b> <b>maximum = 0xFF</b> <b>step = 1</b> <b>default = 0</b>	Defines the WiFi CDB SAR Tx Power Limit - 8bit unsigned with 5bit integer and 3bit fractional. 0x00 = 0b00000000 = 0.125dB; 0xFF = 0b11111111 = 31.875dB. Each step is equivalent to 0.125dB
SAR CDB 5470-5725 MHz Set3 Chain A		<b>minimum = 0</b> <b>maximum = 0xFF</b> <b>step = 1</b> <b>default = 0</b>	Defines the WiFi CDB SAR Tx Power Limit - 8bit unsigned with 5bit integer and 3bit fractional. 0x00 = 0b00000000 = 0.125dB; 0xFF = 0b11111111 = 31.875dB. Each step is equivalent to 0.125dB

SAR CDB 5725-5925 MHz Set3 Chain A	<b>minimum = 0</b> <b>maximum = 0xFF</b> <b>step = 1</b> <b>default = 0</b>	Defines the WiFi CDB SAR Tx Power Limit - 8bit unsigned with 5bit integer and 3bit fractional. 0x00 = 0b00000000 = 0.125dB; 0xFF = 0b11111111 = 31.875dB. Each step is equivalent to 0.125dB
SAR CDB 5945-6165 MHz Set3 Chain A	<b>minimum = 0</b> <b>maximum = 0xFF</b> <b>step = 1</b> <b>default = 0</b>	Defines the WiFi CDB SAR Tx Power Limit - 8bit unsigned with 5bit integer and 3bit fractional. 0x00 = 0b00000000 = 0.125dB; 0xFF = 0b11111111 = 31.875dB. Each step is equivalent to 0.125dB
SAR CDB 6165-6405 MHz Set3 Chain A	<b>minimum = 0</b> <b>maximum = 0xFF</b> <b>step = 1</b> <b>default = 0</b>	Defines the WiFi CDB SAR Tx Power Limit - 8bit unsigned with 5bit integer and 3bit fractional. 0x00 = 0b00000000 = 0.125dB; 0xFF = 0b11111111 = 31.875dB. Each step is equivalent to 0.125dB
SAR CDB 6405-6525 MHz Set3 Chain A	<b>minimum = 0</b> <b>maximum = 0xFF</b> <b>step = 1</b> <b>default = 0</b>	Defines the WiFi CDB SAR Tx Power Limit - 8bit unsigned with 5bit integer and 3bit fractional. 0x00 = 0b00000000 = 0.125dB; 0xFF = 0b11111111 = 31.875dB. Each step is equivalent to 0.125dB
SAR CDB 6525-6705 MHz Set3 Chain A	<b>minimum = 0</b> <b>maximum = 0xFF</b> <b>step = 1</b> <b>default = 0</b>	Defines the WiFi CDB SAR Tx Power Limit - 8bit unsigned with 5bit integer and 3bit fractional. 0x00 = 0b00000000 = 0.125dB; 0xFF = 0b11111111 = 31.875dB. Each step is equivalent to 0.125dB
SAR CDB 6705-6865 MHz Set3 Chain A	<b>minimum = 0</b> <b>maximum = 0xFF</b> <b>step = 1</b> <b>default = 0</b>	Defines the WiFi CDB SAR Tx Power Limit - 8bit unsigned with 5bit integer and 3bit fractional. 0x00 = 0b00000000 = 0.125dB; 0xFF = 0b11111111 = 31.875dB. Each step is equivalent to 0.125dB
SAR CDB 6865-7105 MHz Set3 Chain A	<b>minimum = 0</b> <b>maximum = 0xFF</b> <b>step = 1</b> <b>default = 0</b>	Defines the WiFi CDB SAR Tx Power Limit - 8bit unsigned with 5bit integer and 3bit fractional. 0x00 = 0b00000000 = 0.125dB; 0xFF = 0b11111111 = 31.875dB. Each step is equivalent to 0.125dB
SAR CDB 2400 MHz Set3 Chain B	<b>minimum = 0</b> <b>maximum = 0xFF</b> <b>step = 1</b> <b>default = 0</b>	Defines the WiFi CDB SAR Tx Power Limit - 8bit unsigned with 5bit integer and 3bit fractional. 0x00 = 0b00000000 = 0.125dB; 0xFF = 0b11111111 = 31.875dB. Each step is equivalent to 0.125dB
SAR CDB 5150-5350 MHz Set3 Chain B	<b>minimum = 0</b> <b>maximum = 0xFF</b> <b>step = 1</b>	Defines the WiFi CDB SAR Tx Power Limit - 8bit unsigned with 5bit integer and 3bit fractional. 0x00 =

	<b>default = 0</b>	0b00000000 = 0.125dB; 0xFF = 0b11111111 = 31.875dB. Each step is equivalent to 0.125dB
SAR CDB 5350-5470 MHz Set3 Chain B	<b>minimum = 0</b> <b>maximum = 0xFF</b> <b>step = 1</b> <b>default = 0</b>	Defines the WiFi CDB SAR Tx Power Limit - 8bit unsigned with 5bit integer and 3bit fractional. 0x00 = 0b00000000 = 0.125dB; 0xFF = 0b11111111 = 31.875dB. Each step is equivalent to 0.125dB
SAR CDB 5470-5725 MHz Set3 Chain B	<b>minimum = 0</b> <b>maximum = 0xFF</b> <b>step = 1</b> <b>default = 0</b>	Defines the WiFi CDB SAR Tx Power Limit - 8bit unsigned with 5bit integer and 3bit fractional. 0x00 = 0b00000000 = 0.125dB; 0xFF = 0b11111111 = 31.875dB. Each step is equivalent to 0.125dB
SAR CDB 5725-5925 MHz Set3 Chain B	<b>minimum = 0</b> <b>maximum = 0xFF</b> <b>step = 1</b> <b>default = 0</b>	Defines the WiFi CDB SAR Tx Power Limit - 8bit unsigned with 5bit integer and 3bit fractional. 0x00 = 0b00000000 = 0.125dB; 0xFF = 0b11111111 = 31.875dB. Each step is equivalent to 0.125dB
SAR CDB 5945-6165 MHz Set3 Chain B	<b>minimum = 0</b> <b>maximum = 0xFF</b> <b>step = 1</b> <b>default = 0</b>	Defines the WiFi CDB SAR Tx Power Limit - 8bit unsigned with 5bit integer and 3bit fractional. 0x00 = 0b00000000 = 0.125dB; 0xFF = 0b11111111 = 31.875dB. Each step is equivalent to 0.125dB
SAR CDB 6165-6405 MHz Set3 Chain B	<b>minimum = 0</b> <b>maximum = 0xFF</b> <b>step = 1</b> <b>default = 0</b>	Defines the WiFi CDB SAR Tx Power Limit - 8bit unsigned with 5bit integer and 3bit fractional. 0x00 = 0b00000000 = 0.125dB; 0xFF = 0b11111111 = 31.875dB. Each step is equivalent to 0.125dB
SAR CDB 6405-6525 MHz Set3 Chain B	<b>minimum = 0</b> <b>maximum = 0xFF</b> <b>step = 1</b> <b>default = 0</b>	Defines the WiFi CDB SAR Tx Power Limit - 8bit unsigned with 5bit integer and 3bit fractional. 0x00 = 0b00000000 = 0.125dB; 0xFF = 0b11111111 = 31.875dB. Each step is equivalent to 0.125dB
SAR CDB 6525-6705 MHz Set3 Chain B	<b>minimum = 0</b> <b>maximum = 0xFF</b> <b>step = 1</b> <b>default = 0</b>	Defines the WiFi CDB SAR Tx Power Limit - 8bit unsigned with 5bit integer and 3bit fractional. 0x00 = 0b00000000 = 0.125dB; 0xFF = 0b11111111 = 31.875dB. Each step is equivalent to 0.125dB
SAR CDB 6705-6865 MHz Set3 Chain B	<b>minimum = 0</b> <b>maximum = 0xFF</b> <b>step = 1</b> <b>default = 0</b>	Defines the WiFi CDB SAR Tx Power Limit - 8bit unsigned with 5bit integer and 3bit fractional. 0x00 = 0b00000000 = 0.125dB; 0xFF = 0b11111111 = 31.875dB. Each step is equivalent to 0.125dB

SAR CDB 6865-7105 MHz Set3 Chain B	<b>minimum = 0</b> <b>maximum = 0xFF</b> <b>step = 1</b> <b>default = 0</b>	Defines the WiFi CDB SAR Tx Power Limit - 8bit unsigned with 5bit integer and 3bit fractional. 0x00 = 0b00000000 = 0.125dB; 0xFF = 0b11111111 = 31.875dB. Each step is equivalent to 0.125dB
SAR CDB 2400 MHz Set4 Chain A	<b>minimum = 0</b> <b>maximum = 0xFF</b> <b>step = 1</b> <b>default = 0</b>	Defines the WiFi CDB SAR Tx Power Limit - 8bit unsigned with 5bit integer and 3bit fractional. 0x00 = 0b00000000 = 0.125dB; 0xFF = 0b11111111 = 31.875dB. Each step is equivalent to 0.125dB
SAR CDB 5150-5350 MHz Set4 Chain A	<b>minimum = 0</b> <b>maximum = 0xFF</b> <b>step = 1</b> <b>default = 0</b>	Defines the WiFi CDB SAR Tx Power Limit - 8bit unsigned with 5bit integer and 3bit fractional. 0x00 = 0b00000000 = 0.125dB; 0xFF = 0b11111111 = 31.875dB. Each step is equivalent to 0.125dB
SAR CDB 5350-5470 MHz Set4 Chain A	<b>minimum = 0</b> <b>maximum = 0xFF</b> <b>step = 1</b> <b>default = 0</b>	Defines the WiFi CDB SAR Tx Power Limit - 8bit unsigned with 5bit integer and 3bit fractional. 0x00 = 0b00000000 = 0.125dB; 0xFF = 0b11111111 = 31.875dB. Each step is equivalent to 0.125dB
SAR CDB 5470-5725 MHz Set4 Chain A	<b>minimum = 0</b> <b>maximum = 0xFF</b> <b>step = 1</b> <b>default = 0</b>	Defines the WiFi CDB SAR Tx Power Limit - 8bit unsigned with 5bit integer and 3bit fractional. 0x00 = 0b00000000 = 0.125dB; 0xFF = 0b11111111 = 31.875dB. Each step is equivalent to 0.125dB
SAR CDB 5725-5925 MHz Set4 Chain A	<b>minimum = 0</b> <b>maximum = 0xFF</b> <b>step = 1</b> <b>default = 0</b>	Defines the WiFi CDB SAR Tx Power Limit - 8bit unsigned with 5bit integer and 3bit fractional. 0x00 = 0b00000000 = 0.125dB; 0xFF = 0b11111111 = 31.875dB. Each step is equivalent to 0.125dB
SAR CDB 5945-6165 MHz Set4 Chain A	<b>minimum = 0</b> <b>maximum = 0xFF</b> <b>step = 1</b> <b>default = 0</b>	Defines the WiFi CDB SAR Tx Power Limit - 8bit unsigned with 5bit integer and 3bit fractional. 0x00 = 0b00000000 = 0.125dB; 0xFF = 0b11111111 = 31.875dB. Each step is equivalent to 0.125dB
SAR CDB 6165-6405 MHz Set4 Chain A	<b>minimum = 0</b> <b>maximum = 0xFF</b> <b>step = 1</b> <b>default = 0</b>	Defines the WiFi CDB SAR Tx Power Limit - 8bit unsigned with 5bit integer and 3bit fractional. 0x00 = 0b00000000 = 0.125dB; 0xFF = 0b11111111 = 31.875dB. Each step is equivalent to 0.125dB
SAR CDB 6405-6525 MHz Set4 Chain A	<b>minimum = 0</b> <b>maximum = 0xFF</b> <b>step = 1</b>	Defines the WiFi CDB SAR Tx Power Limit - 8bit unsigned with 5bit integer and 3bit fractional. 0x00 =

		<b>default = 0</b>	0b00000000 = 0.125dB; 0xFF = 0b11111111 = 31.875dB. Each step is equivalent to 0.125dB
SAR CDB 6525-6705 MHz Set4 Chain A		<b>minimum = 0 maximum = 0xFF step = 1 default = 0</b>	Defines the WiFi CDB SAR Tx Power Limit - 8bit unsigned with 5bit integer and 3bit fractional. 0x00 = 0b00000000 = 0.125dB; 0xFF = 0b11111111 = 31.875dB. Each step is equivalent to 0.125dB
SAR CDB 6705-6865 MHz Set4 Chain A		<b>minimum = 0 maximum = 0xFF step = 1 default = 0</b>	Defines the WiFi CDB SAR Tx Power Limit - 8bit unsigned with 5bit integer and 3bit fractional. 0x00 = 0b00000000 = 0.125dB; 0xFF = 0b11111111 = 31.875dB. Each step is equivalent to 0.125dB
SAR CDB 6865-7105 MHz Set4 Chain A		<b>minimum = 0 maximum = 0xFF step = 1 default = 0</b>	Defines the WiFi CDB SAR Tx Power Limit - 8bit unsigned with 5bit integer and 3bit fractional. 0x00 = 0b00000000 = 0.125dB; 0xFF = 0b11111111 = 31.875dB. Each step is equivalent to 0.125dB
SAR CDB 2400 MHz Set4 Chain B		<b>minimum = 0 maximum = 0xFF step = 1 default = 0</b>	Defines the WiFi CDB SAR Tx Power Limit - 8bit unsigned with 5bit integer and 3bit fractional. 0x00 = 0b00000000 = 0.125dB; 0xFF = 0b11111111 = 31.875dB. Each step is equivalent to 0.125dB
SAR CDB 5150-5350 MHz Set4 Chain B		<b>minimum = 0 maximum = 0xFF step = 1 default = 0</b>	Defines the WiFi CDB SAR Tx Power Limit - 8bit unsigned with 5bit integer and 3bit fractional. 0x00 = 0b00000000 = 0.125dB; 0xFF = 0b11111111 = 31.875dB. Each step is equivalent to 0.125dB
SAR CDB 5350-5470 MHz Set4 Chain B		<b>minimum = 0 maximum = 0xFF step = 1 default = 0</b>	Defines the WiFi CDB SAR Tx Power Limit - 8bit unsigned with 5bit integer and 3bit fractional. 0x00 = 0b00000000 = 0.125dB; 0xFF = 0b11111111 = 31.875dB. Each step is equivalent to 0.125dB
SAR CDB 5470-5725 MHz Set4 Chain B		<b>minimum = 0 maximum = 0xFF step = 1 default = 0</b>	Defines the WiFi CDB SAR Tx Power Limit - 8bit unsigned with 5bit integer and 3bit fractional. 0x00 = 0b00000000 = 0.125dB; 0xFF = 0b11111111 = 31.875dB. Each step is equivalent to 0.125dB
SAR CDB 5725-5925 MHz Set4 Chain B		<b>minimum = 0 maximum = 0xFF step = 1 default = 0</b>	Defines the WiFi CDB SAR Tx Power Limit - 8bit unsigned with 5bit integer and 3bit fractional. 0x00 = 0b00000000 = 0.125dB; 0xFF = 0b11111111 = 31.875dB. Each step is equivalent to 0.125dB

SAR CDB 5945-6165 MHz Set4 Chain B	<b>minimum = 0</b> <b>maximum = 0xFF</b> <b>step = 1</b> <b>default = 0</b>	Defines the WiFi CDB SAR Tx Power Limit - 8bit unsigned with 5bit integer and 3bit fractional. 0x00 = 0b00000000 = 0.125dB; 0xFF = 0b11111111 = 31.875dB. Each step is equivalent to 0.125dB
SAR CDB 6165-6405 MHz Set4 Chain B	<b>minimum = 0</b> <b>maximum = 0xFF</b> <b>step = 1</b> <b>default = 0</b>	Defines the WiFi CDB SAR Tx Power Limit - 8bit unsigned with 5bit integer and 3bit fractional. 0x00 = 0b00000000 = 0.125dB; 0xFF = 0b11111111 = 31.875dB. Each step is equivalent to 0.125dB
SAR CDB 6405-6525 MHz Set4 Chain B	<b>minimum = 0</b> <b>maximum = 0xFF</b> <b>step = 1</b> <b>default = 0</b>	Defines the WiFi CDB SAR Tx Power Limit - 8bit unsigned with 5bit integer and 3bit fractional. 0x00 = 0b00000000 = 0.125dB; 0xFF = 0b11111111 = 31.875dB. Each step is equivalent to 0.125dB
SAR CDB 6525-6705 MHz Set4 Chain B	<b>minimum = 0</b> <b>maximum = 0xFF</b> <b>step = 1</b> <b>default = 0</b>	Defines the WiFi CDB SAR Tx Power Limit - 8bit unsigned with 5bit integer and 3bit fractional. 0x00 = 0b00000000 = 0.125dB; 0xFF = 0b11111111 = 31.875dB. Each step is equivalent to 0.125dB
SAR CDB 6705-6865 MHz Set4 Chain B	<b>minimum = 0</b> <b>maximum = 0xFF</b> <b>step = 1</b> <b>default = 0</b>	Defines the WiFi CDB SAR Tx Power Limit - 8bit unsigned with 5bit integer and 3bit fractional. 0x00 = 0b00000000 = 0.125dB; 0xFF = 0b11111111 = 31.875dB. Each step is equivalent to 0.125dB
SAR CDB 6865-7105 MHz Set4 Chain B	<b>minimum = 0</b> <b>maximum = 0xFF</b> <b>step = 1</b> <b>default = 0</b>	Defines the WiFi CDB SAR Tx Power Limit - 8bit unsigned with 5bit integer and 3bit fractional. 0x00 = 0b00000000 = 0.125dB; 0xFF = 0b11111111 = 31.875dB. Each step is equivalent to 0.125dB
Antenna A Current Set	<b>[Default OTP table]</b> [Set 1] [Set 2] [Set 3] [Set 4]	Current Set to be used 0 :Default OTP table 1-3 SAR Sets
Antenna B Current Set	<b>[Default OTP table]</b> [Set 1] [Set 2] [Set 3] [Set 4]	Current Set to be used 0 :Default OTP table 1-3 SAR Sets
WGDS Package	No options	WGDS Package
SAR 2400 MHz Max Allowed for Group 1 (FCC)	<b>minimum = 0</b> <b>maximum = 0xFF</b> <b>step = 1</b>	Defines the WiFi SAR Delta Value to be applied - 8bit unsigned with 5bit integer and 3bit fractional. 0x00 =

	<b>default = 0xFF</b>	0b00000000 = 0.125dB; 0xFF = 0b11111111 = 31.875dB. Each step is equivalent to 0.125dB
SAR 2400 MHz Chain A Offset for Group 1 (FCC)	<b>minimum = 0 maximum = 0xFF step = 1 default = 0</b>	Defines the WiFi SAR Delta Value to be applied - 8bit unsigned with 5bit integer and 3bit fractional. 0x00 = 0b00000000 = 0.125dB; 0xFF = 0b11111111 = 31.875dB. Each step is equivalent to 0.125dB
SAR 2400 MHz Chain B Offset for Group 1 (FCC)	<b>minimum = 0 maximum = 0xFF step = 1 default = 0</b>	Defines the WiFi SAR Delta Value to be applied - 8bit unsigned with 5bit integer and 3bit fractional. 0x00 = 0b00000000 = 0.125dB; 0xFF = 0b11111111 = 31.875dB. Each step is equivalent to 0.125dB
SAR 5200 MHz Max Allowed for Group 1 (FCC)	<b>minimum = 0 maximum = 0xFF step = 1 default = 0xFF</b>	Defines the WiFi SAR Delta Value to be applied - 8bit unsigned with 5bit integer and 3bit fractional. 0x00 = 0b00000000 = 0.125dB; 0xFF = 0b11111111 = 31.875dB. Each step is equivalent to 0.125dB
SAR 5200 MHz Chain A Offset for Group 1 (FCC)	<b>minimum = 0 maximum = 0xFF step = 1 default = 0</b>	Defines the WiFi SAR Delta Value to be applied - 8bit unsigned with 5bit integer and 3bit fractional. 0x00 = 0b00000000 = 0.125dB; 0xFF = 0b11111111 = 31.875dB. Each step is equivalent to 0.125dB
SAR 5200 MHz Chain B Offset for Group 1 (FCC)	<b>minimum = 0 maximum = 0xFF step = 1 default = 0</b>	Defines the WiFi SAR Tx Power Limit - 8bit unsigned with 5bit integer and 3bit fractional. 0x00 = 0b00000000 = 0.125dB; 0xFF = 0b11111111 = 31.875dB. Each step is equivalent to 0.125dB
SAR 6000-7000 MHz Max Allowed for Group 1 (FCC)	<b>minimum = 0 maximum = 0xFF step = 1 default = 0xFF</b>	Defines the WiFi SAR Delta Value to be applied - 8bit unsigned with 5bit integer and 3bit fractional. 0x00 = 0b00000000 = 0.125dB; 0xFF = 0b11111111 = 31.875dB. Each step is equivalent to 0.125dB
SAR 6000-7000 MHz Chain A Offset for Group 1 (FCC)	<b>minimum = 0 maximum = 0xFF step = 1 default = 0</b>	Defines the WiFi SAR Delta Value to be applied - 8bit unsigned with 5bit integer and 3bit fractional. 0x00 = 0b00000000 = 0.125dB; 0xFF = 0b11111111 = 31.875dB. Each step is equivalent to 0.125dB
SAR 6000-7000 MHz Chain B Offset for Group 1 (FCC)	<b>minimum = 0 maximum = 0xFF step = 1 default = 0</b>	Defines the WiFi SAR Tx Power Limit - 8bit unsigned with 5bit integer and 3bit fractional. 0x00 = 0b00000000 = 0.125dB; 0xFF = 0b11111111 = 31.875dB. Each step is equivalent to 0.125dB

SAR 2400 MHz Max Allowed for Group 2 (EU Japan)	<b>minimum = 0</b> <b>maximum = 0xFF</b> <b>step = 1</b> <b>default = 0xFF</b>	Defines the WiFi SAR Delta Value to be applied - 8bit unsigned with 5bit integer and 3bit fractional. 0x00 = 0b00000000 = 0.125dB; 0xFF = 0b11111111 = 31.875dB. Each step is equivalent to 0.125dB
SAR 2400 MHz Chain A Offset for Group 2 (EU Japan)	<b>minimum = 0</b> <b>maximum = 0xFF</b> <b>step = 1</b> <b>default = 0</b>	Defines the WiFi SAR Delta Value to be applied - 8bit unsigned with 5bit integer and 3bit fractional. 0x00 = 0b00000000 = 0.125dB; 0xFF = 0b11111111 = 31.875dB. Each step is equivalent to 0.125dB
SAR 2400 MHz Chain B Offset for Group 2 (EU Japan)	<b>minimum = 0</b> <b>maximum = 0xFF</b> <b>step = 1</b> <b>default = 0</b>	Defines the WiFi SAR Delta Value to be applied - 8bit unsigned with 5bit integer and 3bit fractional. 0x00 = 0b00000000 = 0.125dB; 0xFF = 0b11111111 = 31.875dB. Each step is equivalent to 0.125dB
SAR 5200 MHz Max Allowed for Group 2 (EU Japan)	<b>minimum = 0</b> <b>maximum = 0xFF</b> <b>step = 1</b> <b>default = 0xFF</b>	Defines the WiFi SAR Delta Value to be applied - 8bit unsigned with 5bit integer and 3bit fractional. 0x00 = 0b00000000 = 0.125dB; 0xFF = 0b11111111 = 31.875dB. Each step is equivalent to 0.125dB
SAR 5200 MHz Chain A Offset for Group 2 (EU Japan)	<b>minimum = 0</b> <b>maximum = 0xFF</b> <b>step = 1</b> <b>default = 0</b>	Defines the WiFi SAR Delta Value to be applied - 8bit unsigned with 5bit integer and 3bit fractional. 0x00 = 0b00000000 = 0.125dB; 0xFF = 0b11111111 = 31.875dB. Each step is equivalent to 0.125dB
SAR 5200 MHz Chain B Offset for Group 2 (EU Japan)	<b>minimum = 0</b> <b>maximum = 0xFF</b> <b>step = 1</b> <b>default = 0</b>	Defines the WiFi SAR Delta Value to be applied - 8bit unsigned with 5bit integer and 3bit fractional. 0x00 = 0b00000000 = 0.125dB; 0xFF = 0b11111111 = 31.875dB. Each step is equivalent to 0.125dB
SAR 6000-7000 MHz Max Allowed for Group 2 (EU Japan)	<b>minimum = 0</b> <b>maximum = 0xFF</b> <b>step = 1</b> <b>default = 0xFF</b>	Defines the WiFi SAR Delta Value to be applied - 8bit unsigned with 5bit integer and 3bit fractional. 0x00 = 0b00000000 = 0.125dB; 0xFF = 0b11111111 = 31.875dB. Each step is equivalent to 0.125dB
SAR 6000-7000 MHz Chain A Offset for Group 2 (EU Japan)	<b>minimum = 0</b> <b>maximum = 0xFF</b> <b>step = 1</b> <b>default = 0</b>	Defines the WiFi SAR Delta Value to be applied - 8bit unsigned with 5bit integer and 3bit fractional. 0x00 = 0b00000000 = 0.125dB; 0xFF = 0b11111111 = 31.875dB. Each step is equivalent to 0.125dB
SAR 6000-7000 MHz Chain B Offset for Group 2 (EU Japan)	<b>minimum = 0</b> <b>maximum = 0xFF</b> <b>step = 1</b>	Defines the WiFi SAR Tx Power Limit - 8bit unsigned with 5bit integer and 3bit fractional. 0x00 = 0b00000000 =

		<b>default = 0</b>	0.125dB; 0xFF = 0b11111111 = 31.875dB. Each step is equivalent to 0.125dB
SAR 2400 MHz Max Allowed for Group 3 (ROW)		<b>minimum = 0</b> <b>maximum = 0xFF</b> <b>step = 1</b> <b>default = 0xFF</b>	Defines the WiFi SAR Delta Value to be applied - 8bit unsigned with 5bit integer and 3bit fractional. 0x00 = 0b00000000 = 0.125dB; 0xFF = 0b11111111 = 31.875dB. Each step is equivalent to 0.125dB
SAR 2400 MHz Chain A Offset for Group 3 (ROW)		<b>minimum = 0</b> <b>maximum = 0xFF</b> <b>step = 1</b> <b>default = 0</b>	Defines the WiFi SAR Delta Value to be applied - 8bit unsigned with 5bit integer and 3bit fractional. 0x00 = 0b00000000 = 0.125dB; 0xFF = 0b11111111 = 31.875dB. Each step is equivalent to 0.125dB
SAR 2400 MHz Chain B Offset for Group 3 (ROW)		<b>minimum = 0</b> <b>maximum = 0xFF</b> <b>step = 1</b> <b>default = 0</b>	Defines the WiFi SAR Delta Value to be applied - 8bit unsigned with 5bit integer and 3bit fractional. 0x00 = 0b00000000 = 0.125dB; 0xFF = 0b11111111 = 31.875dB. Each step is equivalent to 0.125dB
SAR 5200 MHz Max Allowed for Group 3 (ROW)		<b>minimum = 0</b> <b>maximum = 0xFF</b> <b>step = 1</b> <b>default = 0xFF</b>	Defines the WiFi SAR Delta Value to be applied - 8bit unsigned with 5bit integer and 3bit fractional. 0x00 = 0b00000000 = 0.125dB; 0xFF = 0b11111111 = 31.875dB. Each step is equivalent to 0.125dB
SAR 5200 MHz Chain A Offset for Group 3 (ROW)		<b>minimum = 0</b> <b>maximum = 0xFF</b> <b>step = 1</b> <b>default = 0</b>	Defines the WiFi SAR Delta Value to be applied - 8bit unsigned with 5bit integer and 3bit fractional. 0x00 = 0b00000000 = 0.125dB; 0xFF = 0b11111111 = 31.875dB. Each step is equivalent to 0.125dB
SAR 5200 MHz Chain B Offset for Group 3 (ROW)		<b>minimum = 0</b> <b>maximum = 0xFF</b> <b>step = 1</b> <b>default = 0</b>	Defines the WiFi SAR Tx Power Limit - 8bit unsigned with 5bit integer and 3bit fractional. 0x00 = 0b00000000 = 0.125dB; 0xFF = 0b11111111 = 31.875dB. Each step is equivalent to 0.125d
SAR 6000-7000 MHz Max Allowed for Group 3 (ROW)		<b>minimum = 0</b> <b>maximum = 0xFF</b> <b>step = 1</b> <b>default = 0xFF</b>	Defines the WiFi SAR Delta Value to be applied - 8bit unsigned with 5bit integer and 3bit fractional. 0x00 = 0b00000000 = 0.125dB; 0xFF = 0b11111111 = 31.875dB. Each step is equivalent to 0.125dB
SAR 6000-7000 MHz Chain A Offset for Group 3 (ROW)		<b>minimum = 0</b> <b>maximum = 0xFF</b> <b>step = 1</b> <b>default = 0</b>	Defines the WiFi SAR Delta Value to be applied - 8bit unsigned with 5bit integer and 3bit fractional. 0x00 = 0b00000000 = 0.125dB; 0xFF = 0b11111111 = 31.875dB. Each step is equivalent to 0.125dB

SAR 6000-7000 MHz Chain B Offset for Group 3 (ROW)	<b>minimum = 0</b> <b>maximum = 0xFF</b> <b>step = 1</b> <b>default = 0</b>	Defines the WiFi SAR Tx Power Limit - 8bit unsigned with 5bit integer and 3bit fractional. 0x00 = 0b00000000 = 0.125dB; 0xFF = 0b11111111 = 31.875dB. Each step is equivalent to 0.125dB
External 32kHz Clock	<b>[Not Valid]</b> [Valid]	This will be used to specify that platform does have valid External 32kHz clock or not..
PPAG Package	No options	PPAG Package
Wifi ANT Gain control	<b>[Disabled]</b> [Enabled]	Enable / Disable WiFi Antenna Gain control.
ANT Gain 2400MHz Chain A	<b>minimum = 0</b> <b>maximum = 0xFF</b> <b>step = 1</b> <b>default = 0x18</b>	Defines the WiFi ANT gain Delta Value to be applied - 8bit signed Two's complement 0.125dB. 0x80 = 0b10000000 = -16dB; 0x7F = 0b01111111 = 15.875dB. Each step is equivalent to 0.125dB
ANT Gain 5150MHz-5350MHz Chain A	<b>minimum = 0</b> <b>maximum = 0xFF</b> <b>step = 1</b> <b>default = 0x28</b>	Defines the WiFi ANT gain Delta Value to be applied - 8bit signed Two's complement 0.125dB. 0x80 = 0b10000000 = -16dB; 0x7F = 0b01111111 = 15.875dB. Each step is equivalent to 0.125dB
Ant Gain 5350MHz-5470MHz Chain A	<b>minimum = 0</b> <b>maximum = 0xFF</b> <b>step = 1</b> <b>default = 0x28</b>	Defines the WiFi ANT gain Delta Value to be applied - 8bit signed Two's complement 0.125dB. 0x80 = 0b10000000 = -16dB; 0x7F = 0b01111111 = 15.875dB. Each step is equivalent to 0.125dB
Ant Gain 5470MHz-5725MHz Chain A	<b>minimum = 0</b> <b>maximum = 0xFF</b> <b>step = 1</b> <b>default = 0x28</b>	Defines the WiFi ANT gain Delta Value to be applied - 8bit signed Two's complement 0.125dB. 0x80 = 0b10000000 = -16dB; 0x7F = 0b01111111 = 15.875dB. Each step is equivalent to 0.125dB
Ant Gain 5725MHz-5945MHz Chain A	<b>minimum = 0</b> <b>maximum = 0xFF</b> <b>step = 1</b> <b>default = 0x28</b>	Defines the WiFi ANT gain Delta Value to be applied - 8bit signed Two's complement 0.125dB. 0x80 = 0b10000000 = -16dB; 0x7F = 0b01111111 = 15.875dB. Each step is equivalent to 0.125dB
Ant Gain 5945MHz-6165MHz Chain A	<b>minimum = 0</b> <b>maximum = 0xFF</b> <b>step = 1</b> <b>default = 0x28</b>	Defines the WiFi ANT gain Delta Value to be applied - 8bit signed Two's complement 0.125dB. 0x80 = 0b10000000 = -16dB; 0x7F = 0b01111111 = 15.875dB. Each step is equivalent to 0.125dB
Ant Gain 6165MHz-6405MHz Chain A	<b>minimum = 0</b> <b>maximum = 0xFF</b>	Defines the WiFi ANT gain Delta Value to be applied - 8bit signed Two's

		<b>step = 1</b> <b>default = 0x28</b>	complement 0.125dB. 0x80 = 0b10000000 = -16dB; 0x7F = 0b01111111 = 15.875dB. Each step is equivalent to 0.125dB
Ant Gain 6405MHZ-6525MHz Chain A		<b>minimum = 0</b> <b>maximum = 0xFF</b> <b>step = 1</b> <b>default = 0x28</b>	Defines the WiFi ANT gain Delta Value to be applied - 8bit signed Two's complement 0.125dB. 0x80 = 0b10000000 = -16dB; 0x7F = 0b01111111 = 15.875dB. Each step is equivalent to 0.125dB
Ant Gain 6525MHZ-6405MHz Chain A		<b>minimum = 0</b> <b>maximum = 0xFF</b> <b>step = 1</b> <b>default = 0x28</b>	Defines the WiFi ANT gain Delta Value to be applied - 8bit signed Two's complement 0.125dB. 0x80 = 0b10000000 = -16dB; 0x7F = 0b01111111 = 15.875dB. Each step is equivalent to 0.125dB
Ant Gain 6705MHZ-6865MHz Chain A		<b>minimum = 0</b> <b>maximum = 0xFF</b> <b>step = 1</b> <b>default = 0x28</b>	Defines the WiFi ANT gain Delta Value to be applied - 8bit signed Two's complement 0.125dB. 0x80 = 0b10000000 = -16dB; 0x7F = 0b01111111 = 15.875dB. Each step is equivalent to 0.125dB
Ant Gain 6865MHZ-7105MHz Chain A		<b>minimum = 0</b> <b>maximum = 0xFF</b> <b>step = 1</b> <b>default = 0x28</b>	Defines the WiFi ANT gain Delta Value to be applied - 8bit signed Two's complement 0.125dB. 0x80 = 0b10000000 = -16dB; 0x7F = 0b01111111 = 15.875dB. Each step is equivalent to 0.125dB
Ant Gain 2400MHz Chain B		<b>minimum = 0</b> <b>maximum = 0xFF</b> <b>step = 1</b> <b>default = 0x18</b>	Defines the WiFi ANT gain Delta Value to be applied - 8bit signed Two's complement 0.125dB. 0x80 = 0b10000000 = -16dB; 0x7F = 0b01111111 = 15.875dB. Each step is equivalent to 0.125dB
Ant Gain 5150MHz-5350MHz Chain B		<b>minimum = 0</b> <b>maximum = 0xFF</b> <b>step = 1</b> <b>default = 0x28</b>	Defines the WiFi ANT gain Delta Value to be applied - 8bit signed Two's complement 0.125dB. 0x80 = 0b10000000 = -16dB; 0x7F = 0b01111111 = 15.875dB. Each step is equivalent to 0.125dB
Ant Gain 5350MHz-5470MHz Chain B		<b>minimum = 0</b> <b>maximum = 0xFF</b> <b>step = 1</b> <b>default = 0x28</b>	Defines the WiFi ANT gain Delta Value to be applied - 8bit signed Two's complement 0.125dB. 0x80 = 0b10000000 = -16dB; 0x7F = 0b01111111 = 15.875dB. Each step is equivalent to 0.125dB
Ant Gain 5470MHz-5725MHz Chain B		<b>minimum = 0</b> <b>maximum = 0xFF</b> <b>step = 1</b> <b>default = 0x28</b>	Defines the WiFi ANT gain Delta Value to be applied - 8bit signed Two's complement 0.125dB. 0x80 = 0b10000000 = -16dB; 0x7F = 0b01111111 = 15.875dB. Each step is equivalent to 0.125dB

		0b01111111 = 15.875dB. Each step is equivalent to 0.125dB
Ant Gain 5725MHZ-5945MHz Chain B	<b>minimum = 0</b> <b>maximum = 0xFF</b> <b>step = 1</b> <b>default = 0x28</b>	Defines the WiFi ANT gain Delta Value to be applied - 8bit signed Two's complement 0.125dB. 0x80 = 0b10000000 = -16dB; 0x7F = 0b01111111 = 15.875dB. Each step is equivalent to 0.125dB
Ant Gain 5945MHZ-6165MHz Chain B	<b>minimum = 0</b> <b>maximum = 0xFF</b> <b>step = 1</b> <b>default = 0x28</b>	Defines the WiFi ANT gain Delta Value to be applied - 8bit signed Two's complement 0.125dB. 0x80 = 0b10000000 = -16dB; 0x7F = 0b01111111 = 15.875dB. Each step is equivalent to 0.125dB
Ant Gain 6165MHZ-6405MHz Chain B	<b>minimum = 0</b> <b>maximum = 0xFF</b> <b>step = 1</b> <b>default = 0x28</b>	Defines the WiFi ANT gain Delta Value to be applied - 8bit signed Two's complement 0.125dB. 0x80 = 0b10000000 = -16dB; 0x7F = 0b01111111 = 15.875dB. Each step is equivalent to 0.125dB
Ant Gain 6405MHZ-6525MHz Chain B	<b>minimum = 0</b> <b>maximum = 0xFF</b> <b>step = 1</b> <b>default = 0x28</b>	Defines the WiFi ANT gain Delta Value to be applied - 8bit signed Two's complement 0.125dB. 0x80 = 0b10000000 = -16dB; 0x7F = 0b01111111 = 15.875dB. Each step is equivalent to 0.125dB
Ant Gain 6525MHZ-6705MHz Chain B	<b>minimum = 0</b> <b>maximum = 0xFF</b> <b>step = 1</b> <b>default = 0x28</b>	Defines the WiFi ANT gain Delta Value to be applied - 8bit signed Two's complement 0.125dB. 0x80 = 0b10000000 = -16dB; 0x7F = 0b01111111 = 15.875dB. Each step is equivalent to 0.125dB
Ant Gain 6705MHZ-6865MHz Chain B	<b>minimum = 0</b> <b>maximum = 0xFF</b> <b>step = 1</b> <b>default = 0x28</b>	Defines the WiFi ANT gain Delta Value to be applied - 8bit signed Two's complement 0.125dB. 0x80 = 0b10000000 = -16dB; 0x7F = 0b01111111 = 15.875dB. Each step is equivalent to 0.125dB
Ant Gain 6865MHZ-7105MHz Chain B	<b>minimum = 0</b> <b>maximum = 0xFF</b> <b>step = 1</b> <b>default = 0x28</b>	Defines the WiFi ANT gain Delta Value to be applied - 8bit signed Two's complement 0.125dB. 0x80 = 0b10000000 = -16dB; 0x7F = 0b01111111 = 15.875dB. Each step is equivalent to 0.125dB
SGOM Package	No Options	SGOM Package
SAR GEO Mapping Mode	<b>[WiFi OTP]</b> [BIOS Information]	Define the SAR GEO mapping mode <u>(Below options will show at this option set BIOS Information)</u>
Default	<b>minimum = 0</b> <b>maximum = 8</b>	Define the SAR Offset group to be assigned to the GEO Profile

		<b>step = 1</b> <b>default = 0</b>	
FCC		<b>minimum = 0</b> <b>maximum = 8</b> <b>step = 1</b> <b>default = 0</b>	Define the SAR Offset group to be assigned to the GEO Profile
TW and alike		<b>minimum = 0</b> <b>maximum = 8</b> <b>step = 1</b> <b>default = 0</b>	Define the SAR Offset group to be assigned to the GEO Profile
Canada ISED		<b>minimum = 0</b> <b>maximum = 8</b> <b>step = 1</b> <b>default = 0</b>	Define the SAR Offset group to be assigned to the GEO Profile
ETSI 5G8SRD		<b>minimum = 0</b> <b>maximum = 8</b> <b>step = 1</b> <b>default = 0</b>	Define the SAR Offset group to be assigned to the GEO Profile
ETSI 5G8Med		<b>minimum = 0</b> <b>maximum = 8</b> <b>step = 1</b> <b>default = 0</b>	Define the SAR Offset group to be assigned to the GEO Profile
Japan		<b>minimum = 0</b> <b>maximum = 8</b> <b>step = 1</b> <b>default = 0</b>	Define the SAR Offset group to be assigned to the GEO Profile
Brazil		<b>minimum = 0</b> <b>maximum = 8</b> <b>step = 1</b> <b>default = 0</b>	Define the SAR Offset group to be assigned to the GEO Profile
ETSI 5G8FCC		<b>minimum = 0</b> <b>maximum = 8</b> <b>step = 1</b> <b>default = 0</b>	Define the SAR Offset group to be assigned to the GEO Profile
Indonesia		<b>minimum = 0</b> <b>maximum = 8</b> <b>step = 1</b> <b>default = 0</b>	Define the SAR Offset group to be assigned to the GEO Profile
South Korea		<b>minimum = 0</b> <b>maximum = 8</b> <b>step = 1</b> <b>default = 0</b>	Define the SAR Offset group to be assigned to the GEO Profile
Chile		<b>minimum = 0</b> <b>maximum = 8</b> <b>step = 1</b> <b>default = 0</b>	Define the SAR Offset group to be assigned to the GEO Profile
ETSI 5G8Pass		<b>minimum = 0</b> <b>maximum = 8</b> <b>step = 1</b>	Define the SAR Offset group to be assigned to the GEO Profile

		<b>default = 0</b>	
Pakistan		<b>minimum = 0</b> <b>maximum = 8</b> <b>step = 1</b> <b>default = 0</b>	Define the SAR Offset group to be assigned to the GEO Profile
Egypt		<b>minimum = 0</b> <b>maximum = 8</b> <b>step = 1</b> <b>default = 0</b>	Define the SAR Offset group to be assigned to the GEO Profile
Tunisia		<b>minimum = 0</b> <b>maximum = 8</b> <b>step = 1</b> <b>default = 0</b>	Define the SAR Offset group to be assigned to the GEO Profile
China BIOS		<b>minimum = 0</b> <b>maximum = 8</b> <b>step = 1</b> <b>default = 0</b>	Define the SAR Offset group to be assigned to the GEO Profile
Russia		<b>minimum = 0</b> <b>maximum = 8</b> <b>step = 1</b> <b>default = 0</b>	Define the SAR Offset group to be assigned to the GEO Profile
EU + ETSI + 5G8SRD		<b>minimum = 0</b> <b>maximum = 8</b> <b>step = 1</b> <b>default = 0</b>	Define the SAR Offset group to be assigned to the GEO Profile
USA Only		<b>minimum = 0</b> <b>maximum = 8</b> <b>step = 1</b> <b>default = 0</b>	Define the SAR Offset group to be assigned to the GEO Profile
EU + ETSI + 5G8DFS		<b>minimum = 0</b> <b>maximum = 8</b> <b>step = 1</b> <b>default = 0</b>	Define the SAR Offset group to be assigned to the GEO Profile
Qatar		<b>minimum = 0</b> <b>maximum = 8</b> <b>step = 1</b> <b>default = 0</b>	Define the SAR Offset group to be assigned to the GEO Profile
External 32kHz Clock		<b>[Not Valid]</b> [Valid]	This will be used to specify that platform does have valid External 32kHz clock or not..
Bluetooth SAR		<b>[Disabled]</b> [Enabled]	Define the mode of SAR control to be used. Disabled: Tx power shall be mandated by device NVM Enabled: Tx power shall be the minimum between BIOS SAR table and BT Device NVM (either Module or Platform)

		(Below options will show at this option set Enabled)
Bluetooth SAR BR	<b>minimum = 0</b> <b>maximum = 0xFF</b> <b>step = 1</b> <b>default = 0</b>	Defines the SAR power restriction for BR Modulation
Bluetooth SAR EDR2	<b>minimum = 0</b> <b>maximum = 0xFF</b> <b>step = 1</b> <b>default = 0</b>	Defines the SAR power restriction for EDR2 Modulation
Bluetooth SAR EDR3	<b>minimum = 0</b> <b>maximum = 0xFF</b> <b>step = 1</b> <b>default = 0</b>	Defines the SAR power restriction for EDR3 Modulation
Bluetooth SAR LE	<b>minimum = 0</b> <b>maximum = 0xFF</b> <b>step = 1</b> <b>default = 0</b>	Defines the SAR power restriction for LE Modulation
Bluetooth SAR LE 2Mhz	<b>minimum = 0</b> <b>maximum = 0xFF</b> <b>step = 1</b> <b>default = 0</b>	Defines the SAR power restriction for LE 2Mhz Modulation
Bluetooth SAR LE LR	<b>minimum = 0</b> <b>maximum = 0xFF</b> <b>step = 1</b> <b>default = 0</b>	Defines the SAR power restriction for LE LR Modulation
Disable SRD Active Channels	<b>minimum = 0</b> <b>maximum = 0x02</b> <b>step = 1</b> <b>default = 0</b>	Enable/Disable SRD Active Channels 00 - ETSI 5.8GHz SRD Active Scan Enable 01 - ETSI 5.8GHz SRD Passive Scan Enable 02 - ETSI 5.8GHz SRD Disabled
Supported Indonesia 5.15-5.35 GHz Band	<b>minimum = 0</b> <b>maximum = 0x02</b> <b>step = 1</b> <b>default = 0</b>	Enable/Disable Indonesia 5.15-5.35 GHz Band 00 - Set 5.115-5.35GHz to Disable in Indonesia 01 - Set 5.115-5.35GHz to Enable (Passive) in Indonesia 02 - Reserved
Ultra High Band Support	<b>minimum = 0</b> <b>maximum = 0x01</b> <b>step = 1</b> <b>default = 0</b>	Enable/Disable UHB support 00 - Disable UHB support 01 - Enable UHB support
Regulatory Configurations	<b>[Disable DRS for China Location]</b> [Enable DRS for China Location]	Enabling DRS for China Location
UART Configurations	<b>[Default]</b>	TBD

UNII-4	<b>minimum = 0</b> <b>maximum = 0xFFFFFFFF</b> <b>step = 1</b> <b>default = 0</b>	Control Enablement UNII-4 over certificate modules Please input HEX value. FCC Bit0 - Apply changes over FCC, UNII-4 setting within module certification (Default Intel module definitions) '0' Work with WiFi FW/OTP definitions '1' Apply changes Bit1 - UNII-4 mode on FCC '0' Disable UNII-4 '1' Enable UNII-4 ETSI Bit2 - Apply changes over ETSI, UNII-4 setting within module certification (Default Intel module definitions) Bit3 - UNII-4 mode on ETSI Bit31:4 - Reserved shall set to zeros
Indoor Control	<b>minimum = 0</b> <b>maximum = 0xFFFFFFFF</b> <b>step = 1</b> <b>default = 0</b>	Device for Indoor Use Only (Solar Family onwards) Please input HEX value. Bit0 - EU Bit1 - Japan Bit2 - China, applied only in case of China BIOS or DRS in China Enabled Bit3 - USA Bit31:4 - Reserved shall set to zeros
WiFi Time Average SAR - WTAS	No Options	WiFi Time Average SAR - WTAS
WTAS Selection	<b>[Disabled]</b> [Enabled]	Enable/Disable WTAS (Below options will show at this option set Enable)
WTAS List Entries	<b>minimum = 0</b> <b>maximum = 0xF</b> <b>step = 1</b> <b>default = 0</b>	No. of blocked countries not approved by OEM to support this feature.
ISO country code to block	<b>minimum = 0</b> <b>maximum = 0xFFFF</b> <b>step = 1</b> <b>default = 0</b>	The decimal equivalent of country code (a two-ASCII-character) as specified in ISO_3166-1. Ex. for JP - 19024
WWAN Configuration	(See Section 2.2.11.1)	Configure WWAN related options

### 2.2.11.1 WWAN Configuration

**Table 2-2-11-1. WWAN Configuration**

BIOS Setting	Options	Description
WWAN Device	[Disabled] <b>[4G - 7360/7560]</b> [5G - M80]	Enable or Disable M.2 WWAN Device (Below options can be set at this option not set Disable)
Firmware Flash Device	[Disabled] <b>[Enabled]</b>	Enable or Disable WWAN Firmware Flash Device
WWAN Reset Workaround	<b>[Disabled]</b> [Enabled]	Enabling this workaroudnd will result in BIOS asserting

		FULL_CARD_POWER_OFF#, PERST# and RESET# WWAN signals before the WWAN Device Power-On Sequence is executed. Disabling it has no impact
WA - WWAN OEM SVID	<b>minimum = 0</b> <b>maximum = 0xFFFF</b> <b>step = 1</b> <b>default = 0x1CF8</b>	WWAN OEM Sub-Vendor ID (This option can be set at WWAN Device set 5G - M80)
WA - WWAN SVID Detect Timeout	<b>minimum = 0</b> <b>maximum = 0xFFFF</b> <b>step = 1</b> <b>default = 0</b>	The timeout value (ms) for detecting WWAN OEM SVID. Please notice it's workaround for OEM only. (This option can be set at WWAN Device set 5G - M80)

## 2.2.12 Power & Performance

**Table 2-2-12 Power & Performance**

BIOS Setting	Options	Description
Power & Performance		
CPU - Power Management Control	(See Section 2.2.12.1)	CPU - Power Management Control Options
GT - Power Management Control	(See Section 2.2.12.2)	GT - Power Management Control Options
Intel(R) Speed Shift Technology Interrupt Control	[Disabled] <b>[Enabled]</b>	Enable/Disable Intel(R) Speed Shift Technology Interrupts

### 2.2.12.1 CPU - Power Management Control

**Table 2-2-12-1. CPU - Power Management Control**

BIOS Setting	Options	Description
CPU - Power Management Control		
Boot performance mode	[Max Battery] [Max Non-Turbo Performance] <b>[Turbo Performance]</b>	Select the performance state that the BIOS will set starting from reset vector.
Intel(R) SpeedStep(tm)	[Disabled] <b>[Enabled]</b>	Allows more than two frequency ranges to be supported. (Show as <u>SETUP_CPU_FEATURES.EISTAvailable</u> is not 0)
Race To Halt (RTH)	[Disabled] <b>[Enabled]</b>	Enable/Disable Race To Halt feature. RTH will dynamically increase CPU frequency in order to enter pkg C-State faster to reduce overall

		power. (RTH is controlled through MSR 1FC bit 20)
Intel(R) Speed Shift Technology	[Disabled] <b>[Enabled]</b>	Enable/Disable Intel(R) Speed Shift Technology support. Enabling will expose the CPPC v2 interface to allow for hardware controlled P-states. (Show as <u>SETUP_CPU_FEATURES.HwpAvailable</u> is not 0)
Intel(R) Turbo Boost Max Technology 3.0	[Disabled] <b>[Enabled]</b>	Enable/Disable Intel(R) Turbo Boost Max Technology 3.0 support. Disabling will report the maximum ratio of the slowest core in <u>_CPC</u> object
Per Core P State OS control mode	[Disabled] <b>[Enabled]</b>	For RKL only. Enable/Disable Per Core P state OS control mode. Disabling will set Bit 31 = 1 command 0x06. When set, the highest core request is used for all other core requests.
HwP Autonomous Per Core P State	[Disabled] <b>[Enabled]</b>	For RKL only. Disable Autonomous PCPS (Bit 30 = 1, command 0x11) Autonomous will request the same value for all cores all the time. Enable PCPS (default Bit 30 = 0, command 0x11)
HwP Autonomous EPP Grouping	[Disabled] <b>[Enabled]</b>	For RKL only. Enable EPP grouping (default Bit 29 = 0, command 0x11) Autonomous will request the same values for all cores with same EPP. Disable EPP grouping (Bit 29 = 1, command 0x11) autonomous will not necessarily request same values for all cores with same EPP.
EPB override over PECI	<b>[Disabled]</b> [Enabled]	For RKL only. Enable/Disable EPB override over PECI. Enable by sending pcode command 0x2b, subcommand 0x3 to 1. This will allow OOB EPB PECI override control
HwP Fast MSR Support	[Disabled] <b>[Enabled]</b>	For RKL only. Enable/Disable HwP Fast MSR Support for IA32_HWP_REQUEST MSR.
HwP Lock	[Disabled] <b>[Enabled]</b>	Enable/Disable HWP Lock support in Misc Power Management MSR.
HDC Control	[Disabled] <b>[Enabled]</b>	This option allows HDC configuration. Disabled: Disable HDC Enabled: Can be enabled by OS if OS native support is available.
Turbo Mode	[Disabled] <b>[Enabled]</b>	Enable/Disable processor Turbo Mode (requires Intel Speed Step or Intel Speed Shift to be available and enabled).

		(Display Turbo option only when there is a P state scheme enabled.)
View/Configure Turbo Options	(See Section 2.2.12.1.1)	View/Configure Turbo Options
Config TDP Configurations	(See Section 2.2.12.1.2)	Config TDP Configurations (Show as <u>SETUP CPU FEATURES.ConfigTdpAvailable</u> is not 0)
CPU VR Settings	(See Section 2.2.12.1.3)	Configure CPU VR Settings
Platform PL1 Enable	<b>[Disabled]</b> [Enabled]	Enable/Disable Platform Power Limit 1 programming. If this option is enabled, it activates the PL1 value to be used by the processor to limit the average power of given time window. (Below options will show at this option set Enabled)
Platform PL1 Power	<b>minimum = 0</b> <b>maximum = 4095875</b> <b>step = 125</b> <b>default = 0</b>	Platform Power Limit 1 Power in Milli Watts. BIOS will round to the nearest 1/8W when programming. Any value can be programmed between Max and Min Power Limits (specified by PACKAGE_POWER_SKU_MSR). For 12.50W, enter 12500. This setting will act as the new PL1 value for the Package RAPL algorithm.
Platform PL1 Time Window	<b>[0]</b> [1] [2] [3] [4] [5] [6] [7] [8] [10] [12] [14] [16] [20] [24] [28] [32] [40] [48] [56] [64] [80] [96] [112] [128]	Platform Power Limit 1 Time Window value in seconds. The value may vary from 0 to 128. 0 = default values. Indicates the time window over which Platform TDP value should be maintained.
Platform PL2 Enable	<b>[Disabled]</b> [Enabled]	Enable/Disable Platform Power Limit 2 programming. If this option is disabled, BIOS will program the default values for Platform Power Limit 2. (Below options will show at this option set Enabled)
Platform PL2 Power	<b>minimum = 0</b> <b>maximum = 4095875</b> <b>step = 125</b> <b>default = 0</b>	Platform Power Limit 2 Power in Milli Watts. BIOS will round to the nearest 1/8W when programming. Any value can be programmed between Max and Min Power Limits (specified by PACKAGE_POWER_SKU_MSR). For 12.50W, enter 12500. This setting will act as the new PL2 value for the Package RAPL algorithm.
Power Limit 4 Override	<b>[Disabled]</b> [Enabled]	Enable/Disable Power Limit 4 override. If this option is disabled, BIOS will leave the default values for Power Limit 4 (Below options will show at this option set Enabled)

Power Limit 4	<b>minimum = 0</b> <b>maximum = 1023875</b> <b>step = 125</b> <b>default = 0</b>	Power Limit 4 in Milli Watts. BIOS will round to the nearest 1/8W when programming. For 12.50W, enter 12500. If the value is 0, BIOS leaves default value
Power Limit 4 Lock	<b>[Disabled]</b> [Enabled]	Power Limit 4 MSR 601h Lock. When enabled PL4 configurations are locked during OS. When disabled PL4 configuration can be changed during OS.
C states	[Disabled] <b>[Enabled]</b>	Enable/Disable CPU Power Management. Allows CPU to go to C states when it's not 100% utilized. (Show as <u>SETUP_CPU_FEATURES.CxAvailable</u> is not 0)
Enhanced C-states	[Disabled] <b>[Enabled]</b>	Enable/Disable C1E. When enabled, CPU will switch to minimum speed when all cores enter C-State. (Show as <u>SETUP_CPU_FEATURES.CxAvailable</u> is not 0 OR <u>CPU_SETUP.EnableCx</u> is not 0 OR <u>SETUP_CPU_FEATURES.C1EAvailable</u> is not 0)
C-State Auto Demotion	CPU_CFL is defined: [C1] [C3] <b>[C1 and C3]</b>  else: [Disabled] <b>[C1]</b>	Configure C-State Auto Demotion (Show as <u>SETUP_CPU_FEATURES.CxAvailable</u> is not 0 OR <u>CPU_SETUP.EnableCx</u> is not 0)
C-State Un-demotion	CPU_CFL is defined: [C1] [C3] <b>[C1 and C3]</b>  else: [Disabled] <b>[C1]</b>	Configure C-State Un-demotion (Show as <u>SETUP_CPU_FEATURES.CxAvailable</u> is not 0 OR <u>CPU_SETUP.EnableCx</u> is not 0)
Package C-State Demotion	CPU_CFL is defined: <b>[Disabled]</b> [Enabled]  else: [Disabled] <b>[Enabled]</b>	Enable/Disable Pkg C-State Demotion
Package C-State Un-demotion	CPU_CFL is defined: <b>[Disabled]</b> [Enabled]  else: [Disabled] <b>[Enabled]</b>	Enable/Disable Pkg C-State Un-demotion (Show as <u>SETUP_CPU_FEATURES.PkgCStateSupported</u> is 1)
CState Pre-Wake	[Disabled] <b>[Enabled]</b>	Disable - Sets bit 30 of POWER_CTL MSR(0x1FC) to 1 to disable the Cstate Pre-Wake (Show as <u>SETUP_CPU_FEATURES.CxAvailable</u> is not 0 OR

		<i>CPU_SETUP.EnableCx</i> is not 0)
IO MWAIT Redirection	<b>[Disabled]</b> [Enabled]	When set, will map IO_read instructions sent to IO registers PMG_IO_BASE_ADDRBASE+offset to MWAIT(offset) (Show as <i>SETUP_CPU_FEATURES.CxAvailable</i> is not 0 OR <i>CPU_SETUP.EnableCx</i> is not 0)
Package C State Limit	[C0/C1] [C2] [C3] [C6] [C7] [C7S] [C8] [C9] [C10] <b>[Auto]</b>	Maximum Package C State Limit Setting. Cpu Default: Leaves to Factory default value.Auto: Initializes to deepest available Package C State Limit. (This options will show at C states set Enabled.) (Show as <i>SETUP_CPU_FEATURES.CxAvailable</i> is not 0 OR <i>CPU_SETUP.EnableCx</i> is not 0)
C6/C7 Short Latency Control(MSR 0x60B)		
Time Unit	[1 ns] [32 ns] <b>[1024 ns]</b> [32768 ns] [1048576 ns] [33554432 ns]  default: CPU_CFL - [1024ns] else - [32768ns]	Unit of measurement for IRTL value - bits [12:10]
Latency	<b>minimum = 0</b> <b>maximum = 0x3FF</b> <b>step = 1</b> <b>default</b> <b>CPU_CFL - 0x76</b> <b>else - 0x9D</b>	Interrupt Response Time Limit value- bits [9:0], Enter 0-1023
C6/C7 Long Latency Control(MSR 0x60C)		
Time Unit	[1 ns] [32 ns] [1024 ns] [32768 ns] [1048576 ns] [33554432 ns]  default: CPU_CFL - [1024ns] else - [32768ns]	Unit of measurement for IRTL value - bits [12:10]
Latency	<b>minimum = 0</b> <b>maximum = 0x3FF</b> <b>step = 1</b>	Interrupt Response Time Limit value- bits [9:0], Enter 0-1023

	<b>default:</b> <b>CPU_CFL - 0x94</b> <b>else - 0x9D</b>	
C8 Latency Control(MSR 0x633)		
Time Unit	[1 ns] [32 ns] [1024 ns] [32768 ns] [1048576 ns] [33554432 ns]  default: CPU_CFL - [1024ns] else - [32768ns]	Unit of measurement for IRTL value - bits [12:10]
Latency	<b>minimum = 0</b> <b>maximum = 0x3FF</b> <b>step = 1</b>  <b>default:</b> <b>CPU_CFL - 0xFA</b> <b>else - 0x9D</b>	Interrupt Response Time Limit value- bits [9:0], Enter 0-1023
C9 Latency Control(MSR 0x634)		
Time Unit	[1 ns] [32 ns] [1024 ns] [32768 ns] [1048576 ns] [33554432 ns]  default: CPU_CFL - [1024ns] else - [32768ns]	Unit of measurement for IRTL value - bits [12:10]
Latency	<b>minimum = 0</b> <b>maximum = 0x3FF</b> <b>step = 1</b>  <b>default:</b> <b>CPU_CFL - 0x14C</b> <b>else - 0x9D</b>	Interrupt Response Time Limit value- bits [9:0], Enter 0-1023
C10 Latency Control(MSR 0x635)		
Time Unit	[1 ns] [32 ns] [1024 ns] [32768 ns] [1048576 ns] [33554432 ns]  default: CPU_CFL - [1024ns] else - [32768ns]	Unit of measurement for IRTL value - bits [12:10]
Latency	<b>minimum = 0</b> <b>maximum = 0x3FF</b> <b>step = 1</b>  <b>default:</b> <b>CPU_CFL - 0x3F2</b> <b>else - 0x9D</b>	Interrupt Response Time Limit value- bits [9:0], Enter 0-1023

Thermal Monitor	[Disabled] <b>[Enabled]</b>	Enable/Disable Thermal Monitor
Interrupt Redirection Mode Selection	CPU_CFL is defined: [Fixed Priority] [Round robin] [Hash Vector] <b>[PAIR with Fixed Priority]</b> [PAIR with Round robin] [PAIR with Hash Vector]  else: <b>[Fixed Priority]</b> [Round robin] [Hash Vector] [No Change]	Interrupt Redirection Mode Select for Logical Interrupts
Timed MWAIT	<b>[Disabled]</b> [Enabled]	Enable/Disable Timed MWAIT Support (Show as <u>SETUP_CPU_FEATURES.TimedMwaitSupported</u> is not 0)
Custom P-state Table	(See Section 2.2.12.1.4)	Add Custom P-state Table
EC Turbo Control Mode	<b>[Disabled]</b> [Enabled]	Enable/Disable EC Turbo Control mode (Below options will show at this option set Enabled) (Show as <u>SETUP_VOLATILE_DATA.PlatformFlavor</u> is not FlavorMobile AND <u>SETUP_VOLATILE_DATA.PlatformFlavor</u> is not FlavorEmbedded) OR <u>CPU_SETUP.TurboMode</u> is not 0)
AC Brick Capacity	<b>[90W AC Brick]</b> [65W AC Brick] [75W AC Brick]	Specify the AC Brick capacity
EC Polling Period	<b>minimum = 1</b> <b>maximum = 255</b> <b>step = 1</b> <b>default = 1</b>	Count 1 to 255 for a range of 10ms to 2.55 seconds (1 count = 10ms)
EC Guard Band Value	<b>minimum = 0</b> <b>maximum = 20</b> <b>step = 1</b> <b>default = 0</b>	Count 1 to 20 for a range of 1 watt to 20 watts
EC Algorithm Selection	<b>minimum = 1</b> <b>maximum = 10</b> <b>step = 1</b> <b>default = 1</b>	Count 1 to 10 for Algorithm Selection
Energy Performance Gain	<b>[Disabled]</b> [Enabled]	Enable/disable Energy Performance Gain. (Below options can be set at this option set Enabled)

EPG DIMM Idd3N	<b>minimum = 0</b> <b>maximum = 2000</b> <b>step = 1</b> <b>default = 26</b>	Active standby current (Idd3N) in milliamps from datasheet. Must be calculated on a per DIMM basis. (Show as <i>SA_SETUP.EpgEnable</i> is not 0)
EPG DIMM Idd3P	<b>minimum = 0</b> <b>maximum = 2000</b> <b>step = 1</b> <b>default = 11</b>	Active power-down current (Idd3P) in milliamps from datasheet. Must be calculated on a per DIMM basis. (Show as <i>SA_SETUP.EpgEnable</i> is not 0)
Power Limit 3 Settings	(See Section 2.2.12.1.5)	Power Limit 3 Settings
CPU Lock Configuration	(See Section 2.2.12.1.6)	CPU Lock Configuration
Dual Tau Boost	<b>[Disable]</b> [Enable]	Enable Dual Tau Boost feature. This is only applicable for CMLS 35W/65W/125W sku.

### 2.2.12.1.1 View/Configure Turbo Options

**Table 2-2-12-1-1. View/Configure Turbo Options**

BIOS Setting	Options	Description
Current Turbo Settings		
Max Turbo Power Limit	No options	Max Turbo Power Limit
Min Turbo Power Limit	No options	Min Turbo Power Limit
Package TDP Limit	No options	Package Processor Base Power (TDP) Limit
Power Limit 1	No options	Power Limit 1 in Milli Watts. BIOS will round to the nearest 1/8W when programming. 0 = no custom override. For 12.50W, enter 12500. Overclocking SKU: Value must be between Max and Min Power Limits (specified by PACKAGE_POWER_SKU_MSR). Other SKUs: This value must be between Min Power Limit and Processor Base Power (TDP) Limit.
Power Limit 2	No options	Power Limit 2 value in Milli Watts. BIOS will round to the nearest 1/8W when programming. 0 = no custom override. For 12.50W, enter 12500. Processor applies control policies such that the package power does not exceed this limit.
Turbo Ratio Limit Options	No options	View/Configure Turbo Ratio Limit Options
Energy Efficient P-state	[Disabled] <b>[Enabled]</b>	Enable/Disable Energy Efficient P-state feature. When set to 0, will disable access to ENERGY_PERFORMANCE_BIAS MSR and CPUID Function 6 ECX[3] will read 0

		<p>indicating no support for Energy Efficient policy setting. When set to 1 will enable access to ENERGY_PERFORMANCE_BIAS MSR 1B0h and CPUID Function 6 ECX[3] will read 1 indicating Energy Efficient policy setting is supported.</p> <p>(Show as <u>SETUP_CPU_FEATURES.TurboModeAvailable</u> is not 0 OR <u>CPU_SETUP.EnableGv</u> is not 0 AND <u>CPU_SETUP.EnableHwp</u> is not 0 OR <u>SETUP_VOLATILE_DATA.PlatformFlavor</u> is not FlavorUpServer)</p>
Package Power Limit MSR Lock	<b>[Disabled]</b> [Enabled]	<p>Enable/Disable locking of Package Power Limit settings. When enabled, PACKAGE_POWER_LIMIT MSR will be locked and a reset will be required to unlock the register.</p> <p>(Show as <u>SETUP_CPU_FEATURES.TurboModeAvailable</u> is not 0 OR <u>CPU_SETUP.EnableGv</u> is not 0 AND <u>CPU_SETUP.EnableHwp</u> is not 0 OR <u>SETUP_VOLATILE_DATA.PlatformFlavor</u> is not FlavorUpServer)</p>
Power Limit 1 Override	<b>[Disabled]</b> [Enabled]	<p>Enable/Disable Power Limit 1 override. If this option is disabled, BIOS will program the default values for Power Limit 1 and Power Limit 1 Time Window.</p> <p>(Show as <u>SETUP_CPU_FEATURES.ConfigTdpAvailable</u> is not 1)</p>
Power Limit 1	<b>minimum = 0</b> <b>maximum = 4095875</b> <b>step = 125</b> <b>default = 0</b>	<p>Power Limit 1 in Milli Watts. BIOS will round to the nearest 1/8W when programming. 0 = no custom override. For 12.50W, enter 12500. Overclocking SKU: Value must be between Max and Min Power Limits (specified by PACKAGE_POWER_SKU_MSR). Other SKUs: This value must be between Min Power Limit and Processor Base Power (TDP) Limit.</p> <p>(Show as <u>SETUP_CPU_FEATURES.ConfigTdpAvailable</u> is not 1 OR <u>CPU_SETUP.LongDurationPwrLimitOverride</u> is not 0)</p>
Power Limit 1 Time Window	<b>[0]</b> [1][2][3][4][5][6] [7][8][10][12][14][16] [20][24][28][32][40][48] [56][64][80][96][112][128]	<p>Power Limit 1 Time Window value in seconds. The value may vary from 0 to 128. 0 = default value (28 sec for Mobile and 8 sec for Desktop). Defines time window which TDP value should be maintained.</p>

		(Show as <u>SETUP_CPU_FEATURES.ConfigTdpAvailable</u> is not 1 OR <u>CPU_SETUP.LongDurationPwrLimitOverride</u> is not 0)
Power Limit 2 Override	[Disabled] <b>[Enabled]</b>	Enable/Disable Power Limit 2 override. If this option is disabled, BIOS will program the default values for Power Limit 2. (Show as <u>SETUP_CPU_FEATURES.ConfigTdpAvailable</u> is not 1)
Power Limit 2	<b>minimum = 0</b> <b>maximum = 4095875</b> <b>step = 125</b> <b>default = 0</b>	Power Limit 2 value in Milli Watts. BIOS will round to the nearest 1/8W when programming. If the value is 0, BIOS will program this value as 1.25*TDP. For 12.50W, enter 12500. Processor applies control policies such that the package power does not exceed this limit. (Show as <u>SETUP_CPU_FEATURES.ConfigTdpAvailable</u> is not 1 OR <u>CPU_SETUP.PowerLimit2</u> is not 0)
Energy Efficient Turbo	[Disabled] <b>[Enabled]</b>	Enable/Disable Energy Efficient Turbo Feature. This feature will opportunistically lower the turbo frequency to increase efficiency. Recommended only to disable in overlocking situations where turbo frequency must remain constant. Otherwise, leave enabled.

### 2.2.12.1.2 Config TDP Configurations

**Table 2-2-12-1-2. Config TDP Configurations**

BIOS Setting	Options	Description
Config TDP Configurations		
Configurable TDP Boot Mode	SETUP_CPU_FEATURES.CtdpUpSupported is not 1: <b>[Nominal]</b> [Down] [Deactivate]  SETUP_CPU_FEATURES.CtdpDownSupported is not 1: <b>[Nominal]</b> [Up] [Deactivate]  SETUP_CPU_FEATURES.CtdpDownSupported is not 0 OR SETUP_CPU_FEATURES.CtdpUpSupported is not 0: <b>[Nominal]</b> [Down]	Configurable TDP Mode as Nominal/Up/Down/Deactivate TDP selection. Deactivate option will set MSR to Nominal and MMIO to Zero.

	[Up] [Deactivate]	
Configurable TDP Lock	<b>[Disabled]</b> [Enabled]	Configurable TDP Mode Lock sets the Lock bits on TURBO_ACTIVATION_RATIO and CONFIG_TDP_CONTROL. Note: When CTD Lock is enabled Custom ConfigTDP Count will be forced to 1 and Custom ConfigTDP Boot Index will be forced to 0.
CTDP BIOS control	<b>[Disabled]</b> [Enabled]	Enables CTD control via runtime ACPI BIOS methods. This "BIOS only" feature does not require EC or driver support. (Show as <u>CPU_SETUP.ConfigTdpLock</u> is not 1 OR <u>SETUP_DATA.EnableDptf</u> is not 1)
ConfigTDP Levels	No options	ConfigTDP Levels Supported from MSR
ConfigTDP Turbo Activation Ratio	No options	ConfigTDP Turbo Activation Ratio values from MSR
Power Limit 1	No options	Power Limit 1 values from MMIO
Power Limit 2	No options	Power Limit 2 values from MMIO
Custom Settings Nominal		
ConfigTDP Nominal	No options	ConfigTDP Nominal Ratio and TDP from MSR
(Below options can be set at Configurable TDP Lock set Disabled)		
Power Limit 1	<b>minimum = 0</b> <b>maximum = 4095875</b> <b>step = 125</b> <b>default = 0</b>	Power Limit 1 in Milli Watts. BIOS will round to the nearest 1/8W when programming. 0 = no custom override. For 12.50W, enter 12500. Overclocking SKU: Value must be between Max and Min Power Limits (specified by PACKAGE_POWER_SKU_MSR). Other SKUs: This value must be between Min Power Limit and TDP Limit.
Power Limit 2	<b>minimum = 0</b> <b>maximum = 4095875</b> <b>step = 125</b> <b>default = 0</b>	Power Limit 2 value in Milli Watts. BIOS will round to the nearest 1/8W when programming. 0 = no custom override. For 12.50W, enter 12500. Processor applies control policies such that the package power does not exceed this limit.
Power Limit 1 Time Window	<b>[0]</b> [1] [2] [3] [4] [5] [6] [7] [8] [10] [12] [14] [16] [20] [24] [28] [32] [40] [48] [56] [64] [80] [96] [112] [128]	Power Limit 1 Time Window value in seconds. The value may vary from 0 to 128. 0 = default value (28 sec for Mobile and 8 sec for Desktop). Defines time window which TDP value should be maintained.

ConfigTDP Turbo Activation Ratio	<b>minimum = 0</b> <b>maximum = 255</b> <b>step = 1</b> <b>default = 0</b>	Custom value for Turbo Activation Ratio. Needs to be configured with valid values from LFM to Max Turbo. 0 means don't use custom value
Custom Settings Down		(Show as <i>SETUP_CPU_FEATURES.CtdpDownSupported</i> is not 0)
ConfigTDP Level1	No options	ConfigTDP Level1 Ratio and TDP from MSR
<u>(Below options can be set at Configurable TDP Lock set Disabled)</u>		
Power Limit 1	<b>minimum = 0</b> <b>maximum = 4095875</b> <b>step = 125</b> <b>default = 0</b>	Power Limit 1 in Milli Watts. BIOS will round to the nearest 1/8W when programming. 0 = no custom override. For 12.50W, enter 12500. Overclocking SKU: Value must be between Max and Min Power Limits (specified by PACKAGE_POWER_SKU_MSR). Other SKUs: This value must be between Min Power Limit and TDP Limit.
Power Limit 2	<b>minimum = 0</b> <b>maximum = 4095875</b> <b>step = 125</b> <b>default = 0</b>	Power Limit 2 value in Milli Watts. BIOS will round to the nearest 1/8W when programming. 0 = no custom override. For 12.50W, enter 12500. Processor applies control policies such that the package power does not exceed this limit.
Power Limit 1 Time Window	[0] [1] [2] [3] [4] [5] [6] [7] [8] [10] [12] [14] [16] [20] [24] [28] [32] [40] [48] [56] [64] [80] [96] [112] [128]	Power Limit 1 Time Window value in seconds. The value may vary from 0 to 128. 0 = default value (28 sec for Mobile and 8 sec for Desktop). Defines time window which TDP value should be maintained.
ConfigTDP Turbo Activation Ratio	<b>minimum = 0</b> <b>maximum = 255</b> <b>step = 1</b> <b>default = 0</b>	Custom value for Turbo Activation Ratio. Needs to be configured with valid values from LFM to Max Turbo. 0 means don't use custom value
Custom Settings Up		(Show as <i>SETUP_CPU_FEATURES.CtdpUpSupported</i> is not 0)
ConfigTDP Level2	No options	ConfigTDP Level2 Ratio and TDP from MSR
<u>(Below options can be set at Configurable TDP Lock set Disabled)</u>		
Power Limit 1	<b>minimum = 0</b> <b>maximum = 4095875</b> <b>step = 125</b> <b>default = 0</b>	Power Limit 1 in Milli Watts. BIOS will round to the nearest 1/8W when programming. 0 = no custom override. For 12.50W, enter 12500. Overclocking SKU: Value must be between Max and Min Power Limits (specified by PACKAGE_POWER_SKU_MSR). Other SKUs: This value must be between Min Power Limit and TDP Limit.

Power Limit 2	<b>minimum = 0</b> <b>maximum = 4095875</b> <b>step = 125</b> <b>default = 0</b>	Power Limit 2 value in Milli Watts. BIOS will round to the nearest 1/8W when programming. 0 = no custom override. For 12.50W, enter 12500. Processor applies control policies such that the package power does not exceed this limit.
Power Limit 1 Time Window	<b>[0]</b> [1] [2] [3] [4] [5] [6] [7] [8] [10] [12] [14] [16] [20] [24] [28] [32] [40] [48] [56] [64] [80] [96] [112] [128]	Power Limit 1 Time Window value in seconds. The value may vary from 0 to 128. 0 = default value (28 sec for Mobile and 8 sec for Desktop). Defines time window which TDP value should be maintained.
ConfigTDP Turbo Activation Ratio	<b>minimum = 0</b> <b>maximum = 255</b> <b>step = 1</b> <b>default = 0</b>	Custom value for Turbo Activation Ratio. Needs to be configured with valid values from LFM to Max Turbo. 0 means don't use custom value

### 2.2.12.1.3 CPU VR Settings

**Table 2-2-12-1-3. CPU VR Settings**

BIOS Setting	Options	Description
CPU VR Settings		
Current VccIn Aux Icc Max	No Options	Current VccIn Aux Icc Max
PSYS Slope	<b>minimum = 0</b> <b>maximum = 200</b> <b>step = 1</b> <b>default = 0</b>	PSYS Slope defined in 1/100 increments. Range is 0-200. For a 1.25 slope, enter 125. 0 = AUTO. Uses BIOS VR mailbox command 0x9.
PSYS Offset	<b>minimum = 0</b> <b>maximum = 255</b> <b>step = 1</b> <b>default = 0</b>	PSYS Offset defined in 1/1000 increments. Range is 0-63999. For an offset of 25.348, enter 25348. PSYS Uses BIOS VR mailbox command 0x4.
PSYS Prefix	[+] [-]	Sets the offset value as positive or negative.
PSYS PMax Power	<b>minimum = 0</b> <b>maximum = 0x1FFF</b> <b>step = 1</b> <b>default = 0</b>	PSYS PMax power, defined in 1/8 Watt increments. Range 0-8192. For a PMax of 125W, enter 1000. 0 = AUTO. Uses BIOS VR mailbox command 0xB.
Min Voltage Override	[Disabled] [Enabled]	Min Voltage Override. Enable to override minimum voltage for runtime and for C8. <i>(Below will show at this option set to Enable)</i>
Min Voltage Runtime	<b>minimum = 0</b> <b>maximum = 1999</b> <b>step = 1</b> <b>default = 0</b>	Min Voltage for Runtime. Range is 0 - 1999mV in 1/128 volt increments. Input is in mVolts.

Min Voltage C8	<b>minimum = 0</b> <b>maximum = 255</b> <b>step = 1</b> <b>default = 0</b>	Min Voltage for Package C8. Range is 0 - 1999mV in 1/128 volt increments. Input is in mVolts.
VccIn Aux Icc Max	<b>minimum = 0</b> <b>maximum = 512</b> <b>step = 1</b> <b>default = 0</b>	Sets the Max Icc VccIn Aux value defined in 1/4A increments. Range is 0-512. For an IccMax 32A, enter 128(32*4).
VccIn Aux IMON Slope	<b>minimum = 0</b> <b>maximum = 200</b> <b>step = 1</b> <b>default = 1</b>	VccIN Aux IMON Slope defined in 1/100 increments. Range is 0-200. For a 1.25 slope, enter 125. 0 = AUTO. Uses BIOS VR mailbox command 0x18.
VccIN Aux IMON Offset	<b>minimum = 0</b> <b>maximum = 63999</b> <b>step = 1</b> <b>default = 0</b>	VccIN Aux IMON Offset defined in 1/1000 increments. Range is 0-63999. For an offset of 25.348, enter 25348. IMON Uses BIOS VR mailbox command 0x18.
VccIN Aux IMON Prefix	[+] [-]	Sets the offset value as positive or negative.
Vsys Critical	[Disable] [Enable]	Vsys Critical Enable or disable ( <i>Below will show at this option set to Enable</i> )
Vsys Full Scale	<b>minimum = 0</b> <b>maximum = 255</b> <b>step = 1</b> <b>default = 24</b>	Input Vsys Full Scal and Critical Threshold to program Vsys Crit(0x4a). Vsys Crit= Critical Threshold/Full Scale) * 0xFF
Vsys Critical Threshold	<b>minimum = 0</b> <b>maximum = 255</b> <b>step = 1</b> <b>default = 6</b>	Input Vsys Full Scal and Critical Threshold to program Vsys Crit(0x4a). Vsys Crit= Critical Threshold/Full Scale) * 0xFF
Assertion Deglitch Mantissa	<b>minimum = 0</b> <b>maximum = 255</b> <b>step = 1</b> <b>default = 1</b>	Assertion Deglitch Mantissa 0x4F[7-3]. Assertion Deglitch = 2 $\mu$ s * Mantissa * 2^(Exponent)
Assertion Deglitch Exponent	<b>minimum = 0</b> <b>maximum = 255</b> <b>step = 1</b> <b>default = 0</b>	Assertion Deglitch Exponent 0x4F[3-0]. Assertion Deglitch = 2 $\mu$ s * Mantissa * 2^(Exponent)
De assertion Deglitch Mantissa	<b>minimum = 0</b> <b>maximum = 255</b> <b>step = 1</b> <b>default = 13</b>	De Assertion Deglitch Mantissa 0x49[7-3]. Assertion Deglitch = 2 $\mu$ s * Mantissa * 2^(Exponent)
De assertion Deglitch Exponent	<b>minimum = 0</b> <b>maximum = 255</b> <b>step = 1</b> <b>default = 2</b>	De Assertion Deglitch Exponent 0x49[3-0]. Assertion Deglitch = 2 $\mu$ s * Mantissa * 2^(Exponent)
VR Power Delivery Design	[AUTO] [ADL P 282 15W] [ADL P 482 28W]	Specifies the ADL Desktop board design used for the VR settings override values. By default, BIOS will override the default

	<p>[ADL P 682 28W]          [ADL P 682 45W]          [ADL P 142 15W]          [ADL P 242 15W]          [ADL P 482 45W]          [ADL P 442 45W]          [ADL P 442 28W]          [ADL P 282 28W]          [ADL P 242 28W]          [ADL P 142 28W]          [ADL P 242 45W]          [ADL P 182 28W]          [ADL P 662 28W]          [ADL P 642 28W]</p>	<p>Desktop VR settings based on the board design. A value of AUTO(0) will use the board ID to determine the board design. Any other value will override the board id logic to provide a custom VR Power Delivery Design value. This is intended primarily for validation.</p>
Acoustic Noise Settings	(See Section 2.2.12.1.3.1)	Configure Acoustic Noise Settings for IA, GT and SA domains
System Agent VR Settings	(See Section 2.2.12.1.3.2)	Configure System Agent VR Settings (Show as <u>CPU_SETUP_VOLATILE_DATA.SaVrLocked</u> is not 1)
Core/IA VR Settings	(See Section 2.2.12.1.3.3)	Configure Core/IA VR Settings (Show as <u>CPU_SETUP_VOLATILE_DATA.CoreVrLocked</u> is not 1)
GT VR Settings	(See Section 2.2.12.1.3.4)	Configure GT VR Settings (Show as <u>CPU_SETUP_VOLATILE_DATA.GtVrLocked</u> is not 1)
RFI Settings	(See Section 2.2.12.1.3.5)	Configure RFI Settings (Show as <u>SETUP_CPU_FEATURES.McivrSupported</u> is not 0 AND <u>SETUP_CPU_FEATURES.FivrSupported</u> is not 0)

### 2.2.12.1.3.1 Acoustic Noise Settings

**Table 2-2-12-1-3-1. Acoustic Noise Settings**

BIOS Setting	Options	Description
Acoustic Noise Settings		
Acoustic Noise Mitigation	<b>[Disabled]</b> [Enabled]	Enabling this option will help mitigate acoustic noise on certain SKUs when the CPU is in deeper C state. <u>(Below options can be set at this option set Enabled)</u>
Pre Wake Time	<b>minimum = 0</b> <b>maximum = 255</b> <b>step = 1</b> <b>default = 0</b>	Set the maximum Pre Wake randomization time in micro ticks. Range is 0-255. This is for acoustic noise mitigation Dynamic Periodicity Alteration (DPA) tuning.
Ramp Up Time	<b>minimum = 0</b> <b>maximum = 255</b> <b>step = 1</b> <b>default = 0</b>	Set the maximum Ramp Up randomization time in micro ticks. Range is 0-255. This is for acoustic noise mitigation Dynamic Periodicity Alteration (DPA) tuning.
Ramp Down Time	<b>minimum = 0</b> <b>maximum = 255</b> <b>step = 1</b> <b>default = 0</b>	Set the maximum Ramp Down randomization time in micro ticks. Range is 0-255. This is for acoustic noise mitigation Dynamic Periodicity Alteration (DPA) tuning.
IA VR Domain		
Disable Fast PKG C State Ramp for IA Domain	<b>[False]</b> [True]	This option needs to be configured to reduce acoustic noise during deeper C states. False: Don't disable Fast ramp during deeper C states; True: Disable Fast ramp during deeper C state
Slow Slew Rate for IA Domain	<b>[Fast/2]</b> [Fast/4] [Fast/8] [Fast/16]	Set VR IA Slow Slew Rate for Deep Package C State ramp time; Slow slew rate equals to Fast divided by number, the number is 2, 4, 8, 16 to slow down the slew rate to help minimize acoustic noise
GT VR Domain		
Disable Fast PKG C State Ramp for GT Domain	<b>[False]</b> [True]	This option needs to be configured to reduce acoustic noise during deeper C states. False: Don't disable Fast ramp during deeper C states; True: Disable Fast ramp during deeper C state
Slow Slew Rate for GT Domain	<b>[Fast/2]</b> [Fast/4]	Set VR GT Slow Slew Rate for Deep Package C State ramp time; Slow

	[Fast/8] [Fast/16]	slew rate equals to Fast divided by number, the number is 2, 4, 8, 16 to slow down the slew rate to help minimize acoustic noise
SA VR Domain		
Disable Fast PKG C State Ramp for SA Domain	<b>[False]</b> [True]	This option needs to be configured to reduce acoustic noise during deeper C states. False: Don't disable Fast ramp during deeper C states; True: Disable Fast ramp during deeper C state
Slow Slew Rate for SA Domain	<b>[Fast/2]</b> [Fast/4] [Fast/8]	Set VR SA Slow Slew Rate for Deep Package C State ramp time; Slow slew rate equals to Fast divided by number, the number is 2, 4, 8, 16 to slow down the slew rate to help minimize acoustic noise

### 2.2.12.1.3.2 System Agent VR Settings

**Table 2-2-11-1-3-2. System Agent VR Settings**

BIOS Setting	Options	Description
System Agent VR Domain		
VR Config Enable	[Disabled] <b>[Enabled]</b>	VR Config Enable(Below options will show at this option set <u>Enabled</u> )
Current AC Loadline	No Options	Current AC Loadline
Current DC Loadline	No Options	Current DC Loadline
Current Psi1 Threshold	No Options	Current Psi1 Threshold
Current Psi2 Threshold	No Options	Current Psi2 Threshold
Current Psi3 Threshold	No Options	Current Psi3 Threshold
Current Imon Slope	No Options	Current Imon Slope
Current Imon Offset	No Options	Current Imon Offset
Current VR Current Limit	No Options	Current VR Current Limit
Current Tdc Current Limit	No Options	Current Tdc Current Limit
Current Voltage Limit	No Options	Current Voltage Limit
AC Loadline	<b>minimum = 0</b> <b>maximum = 6249</b> <b>step = 0</b> <b>default = 0</b>	AC Loadline defined in 1/100 mOhms. A value of 100 = 1.00 mOhm, and 1255 = 12.55 mOhm. Range is 0-6249 (0-62.49)

		mOhms). 0 = AUTO/HW default. Uses BIOS mailbox command 0x2.
DC Loadline	<b>minimum = 0</b> <b>maximum = 6249</b> <b>step = 0</b> <b>default = 0</b>	DC Loadline defined in 1/100 mOhms. A value of 100 = 1.00 mOhm, and 1255 = 12.55 mOhm. Range is 0-6249 (0-62.49 mOhms). 0 = AUTO/HW default. Uses BIOS mailbox command 0x2.
PS Current Threshold1	<b>minimum = 0</b> <b>maximum = 512</b> <b>step = 1</b> <b>default = 80</b>	PS Current Threshold1, defined in 1/4 A increments. A value of 400 = 100A. Range 0-512, which translates to 0-128A. 0 = AUTO. Uses BIOS VR mailbox command 0x3.
PS Current Threshold2	<b>minimum = 0</b> <b>maximum = 512</b> <b>step = 1</b> <b>default = 20</b>	PS Current Threshold2, defined in 1/4 A increments. A value of 400 = 100A. Range 0-512, which translates to 0-128A. 0=AUTO. Uses BIOS VR mailbox command 0x3.
PS Current Threshold3	<b>minimum = 0</b> <b>maximum = 512</b> <b>step = 1</b> <b>default = 4</b>	PS Current Threshold3, defined in 1/4 A increments. A value of 400 = 100A. Range 0-512, which translates to 0-128A. 0 = AUTO. Uses BIOS VR mailbox command 0x3.
PS3 Enable	[Disabled] <b>[Enabled]</b>	PS3 Enable/Disable. 0 - Disabled, 1 - Enabled. Uses BIOS VR mailbox command 0x3.
PS4 Enable	[Disabled] <b>[Enabled]</b>	PS4 Enable/Disable. 0 - Disabled, 1 - Enabled. Uses BIOS VR mailbox command 0x3
IMON Slope	<b>minimum = 0</b> <b>maximum = 200</b> <b>step = 1</b> <b>default = 0</b>	IMON Slope defined in 1/100 increments. Range is 0-200. For a 1.25 slope, enter 125. 0 = AUTO. Uses BIOS VR mailbox command 0x4.
IMON Offset	<b>minimum = 0</b> <b>maximum = 63999</b> <b>step = 1</b> <b>default = 0</b>	IMON Offset defined in 1/1000 increments. Range is 0-63999. For an offset of 25.348, enter 25348. IMON Uses BIOS VR mailbox command 0x4.
IMON Prefix	<b>[+] [-]</b>	Sets the offset value as positive or negative.
VR Current Limit	<b>minimum = 0</b> <b>maximum = 2048</b> <b>step = 1</b> <b>default = 0</b>	Voltage Regulator Current Limit (Icc Max). This value represents the Maximum instantaneous current allowed at any given time. The value is represented in 1/4 A increments. A value of 400 =

		100A. 0 means AUTO. Uses BIOS VR mailbox command 0x6.
VR Voltage Limit	<b>minimum = 0</b> <b>maximum = 7999</b> <b>step = 1</b> <b>default = 0</b>	VR Voltage Limit, defined in mV. Range is 0-7999mV. For a Voltage Limit of 1.25V, enter 1250. 0 = AUTO. Uses BIOS VR mailbox command 0x6
TDC Enable	<b>[Disabled]</b> [Enabled]	TDC Enable. 0- Disable, 1 - Enable
TDC Current Limit	<b>minimum = 0</b> <b>maximum = 32767</b> <b>step = 125</b> <b>default = 0</b>	TDC Current Limit, defined in 1/8A increments. Range 0-32767. For a TDC Current Limit of 125A, enter 1000. 0 = 0 Amps. Uses BIOS VR mailbox command 0x1A.
TDC Time Window	<b>[1 ms]</b> [2 ms] [3 ms] [4 ms] [5 ms] [6 ms] [7 ms] [8ms] [10ms]	TDC Time Window, value in milliseconds. 1ms is default. Range from 1ms to 10ms, except for 9ms. 9ms has no valid encoding in the MSR definition.
TDC Lock	<b>[Disabled]</b> [Enabled]	TDC Lock

### 2.2.12.1.3.3 Core/IA VR Settings

**Table 2-2-11-1-3-3. Core/IA VR Settings**

BIOS Setting	Options	Description
Core/IA VR Domain		
VR Config Enable	<b>[Disabled]</b> <b>[Enabled]</b>	VR Config Enable (Below options will show at this option set Enabled)
Current AC Loadline	No Options	Current AC Loadline
Current DC Loadline	No Options	Current DC Loadline
Current Psi1 Threshold	No Options	Current Psi1 Threshold
Current Psi2 Threshold	No Options	Current Psi2 Threshold
Current Psi3 Threshold	No Options	Current Psi3 Threshold
Current Imon Slope	No Options	Current Imon Slope
Current Imon Offset	No Options	Current Imon Offset
Current VR Current Limit	No Options	Current VR Current Limit
Current Tdc Current Limit	No Options	Current Tdc Current Limit
Current Voltage Limit	No Options	Current Voltage Limit

AC Loadline	<b>minimum = 0</b> <b>maximum = 62500</b> <b>step = 0</b> <b>default = 0</b>	AC Loadline defined in 1/100 mOhms. A value of 100 = 1.00 mOhm, and 1255 = 12.55 mOhm. Range is 0-6249 (0-62.49 mOhms). 0 = AUTO/HW default. Uses BIOS mailbox command 0x2.
DC Loadline	<b>minimum = 0</b> <b>maximum = 62500</b> <b>step = 0</b> <b>default = 0</b>	DC Loadline defined in 1/100 mOhms. A value of 100 = 1.00 mOhm, and 1255 = 12.55 mOhm. Range is 0-6249 (0-62.49 mOhms). 0 = AUTO/HW default. Uses BIOS mailbox command 0x2.
PS Current Threshold1	<b>minimum = 0</b> <b>maximum = 512</b> <b>step = 1</b> <b>default = 80</b>	PS Current Threshold1, defined in 1/4 A increments. A value of 400 = 100A. Range 0-512, which translates to 0-128A. 0 = AUTO. Uses BIOS VR mailbox command 0x3.
PS Current Threshold2	<b>minimum = 0</b> <b>maximum = 512</b> <b>step = 1</b> <b>default = 20</b>	PS Current Threshold2, defined in 1/4 A increments. A value of 400 = 100A. Range 0-512, which translates to 0-128A. 0 = AUTO. Uses BIOS VR mailbox command 0x3.
PS Current Threshold3	<b>minimum = 0</b> <b>maximum = 512</b> <b>step = 1</b> <b>default = 4</b>	PS Current Threshold3, defined in 1/4 A increments. A value of 400 = 100A. Range 0-512, which translates to 0-128A. 0 = AUTO. Uses BIOS VR mailbox command 0x3.
PS3 Enable	[Disabled] <b>[Enabled]</b>	PS3 Enable/Disable. 0 - Disabled, 1 - Enabled. Uses BIOS VR mailbox command 0x3.
PS4 Enable	[Disabled] <b>[Enabled]</b>	PS4 Enable/Disable. 0 - Disabled, 1 - Enabled. Uses BIOS VR mailbox command 0x3
IMON Slope	<b>minimum = 0</b> <b>maximum = 200</b> <b>step = 1</b> <b>default = 0</b>	IMON Slope defined in 1/100 increments. Range is 0-200. For a 1.25 slope, enter 125. 0 = AUTO. Uses BIOS VR mailbox command 0x4.
IMON Offset	<b>minimum = 0</b> <b>maximum = 63999</b> <b>step = 1</b> <b>default = 0</b>	IMON Offset defined in 1/1000 increments. Range is 0-63999. For an offset of 25.348, enter 25348. IMON Uses BIOS VR mailbox command 0x4.
IMON Prefix	<b>[+] [-]</b>	Sets the offset value as positive or negative.
VR Current Limit	<b>minimum = 0</b> <b>maximum = 2048</b>	Voltage Regulator Current Limit (Icc Max). This value represents

	<b>step = 1</b> <b>default = 0</b>	the Maximum instantaneous current allowed at any given time. The value is represented in 1/4 A increments. A value of 400 = 100A. 0 means AUTO. Uses BIOS VR mailbox command 0x6.
VR Voltage Limit	<b>minimum = 0</b> <b>maximum = 7999</b> <b>step = 1</b> <b>default = 0</b>	Voltage Limit (VMAX). This value represents the Maximum instantaneous voltage allowed at any given time. Range is 0 - 7999mV. Uses BIOS VR mailbox command 0x8.
TDC Enable	[Disabled] <b>[Enabled]</b>	TDC Enable. 0- Disable, 1 - Enable(Below options will show at <u>this option set Enabled</u> )
TDC Current Limit	<b>minimum = 0</b> <b>maximum = 32767</b> <b>step = 125</b> <b>default = 0</b>	TDC Current Limit, defined in 1/8A increments. Range 0-32767. For a TDC Current Limit of 125A, enter 1000. 0 = 0 Amps. Uses BIOS VR mailbox command 0x1A.
TDC Time Window	<b>[1 ms]</b> [2 ms] [3 ms] [4 ms] [5 ms] [6 ms] [7 ms] [8ms] [10ms] [55ms] [156ms] [375ms] [500ms] [750ms] [1sec] [2sec] [3sec] [4sec] [5sec] [6sec] [7sec] [8sec] [10sec] [12sec] [14sec] [16sec] [20sec] [24sec] [28sec] [32sec] [40sec] [48sec] [56sec] [64sec] [80sec] [96sec] [112sec] [128sec] [160sec] [192sec] [224sec] [256sec] [320sec] [384sec] [448sec]	TDC Time Window, value in milliseconds. 1ms is default. Range from 1ms to 10ms, except for 9ms. 9ms has no valid encoding in the MSR definition.
TDC Lock	<b>[Disabled]</b> [Enabled]	TDC Lock
IRMS	<b>[Disabled]</b> [Enabled]	Enable/Disable IRMS - Current root mean square

#### 2.2.12.1.3.4 GT VR Settings

**Table 2-2-12-1-3-4. GT VR Settings**

BIOS Setting	Options	Description
GT Domain		
VR Config Enable	[Disabled] <b>[Enabled]</b>	VR Config Enable (Below options will show at this <u>option set Enabled</u> )
Current AC Loadline	No Options	Current AC Loadline

Current DC Loadline	No Options	Current DC Loadline
Current Psi1 Threshold	No Options	Current Psi1 Threshold
Current Psi2 Threshold	No Options	Current Psi2 Threshold
Current Psi3 Threshold	No Options	Current Psi3 Threshold
Current Imon Slope	No Options	Current Imon Slope
Current Imon Offset	No Options	Current Imon Offset
Current VR Current Limit	No Options	Current VR Current Limit
Current Tdc Current Limit	No Options	Current Tdc Current Limit
Current Voltage Limit	No Options	Current Voltage Limit
AC Loadline	<b>minimum = 0</b> <b>maximum = 62500</b> <b>step = 0</b> <b>default = 0</b>	AC Loadline defined in 1/100 mOhms. A value of 100 = 1.00 mOhm, and 1255 = 12.55 mOhm. Range is 0-6249 (0-62.49 mOhms). 0 = AUTO/HW default. Uses BIOS mailbox command 0x2.
DC Loadline	<b>minimum = 0</b> <b>maximum = 62500</b> <b>step = 0</b> <b>default = 0</b>	DC Loadline defined in 1/100 mOhms. A value of 100 = 1.00 mOhm, and 1255 = 12.55 mOhm. Range is 0-6249 (0-62.49 mOhms). 0 = AUTO/HW default. Uses BIOS mailbox command 0x2.
PS Current Threshold1	<b>minimum = 0</b> <b>maximum = 512</b> <b>step = 1</b> <b>default = 80</b>	PS Current Threshold1, defined in 1/4 A increments. A value of 400 = 100A. Range 0-512, which translates to 0-128A. 0 = AUTO. Uses BIOS VR mailbox command 0x3.
PS Current Threshold2	<b>minimum = 0</b> <b>maximum = 512</b> <b>step = 1</b> <b>default = 20</b>	PS Current Threshold2, defined in 1/4 A increments. A value of 400 = 100A. Range 0-512, which translates to 0-128A. 0 = AUTO. Uses BIOS VR mailbox command 0x3.
PS Current Threshold3	<b>minimum = 0</b> <b>maximum = 512</b> <b>step = 1</b> <b>default = 4</b>	PS Current Threshold3, defined in 1/4 A increments. A value of 400 = 100A. Range 0-512, which translates to 0-128A. 0 = AUTO. Uses BIOS VR mailbox command 0x3.
PS3 Enable	[Disabled] <b>[Enabled]</b>	PS3 Enable/Disable. 0 - Disabled, 1 - Enabled. Uses BIOS VR mailbox command 0x3.

PS4 Enable	[Disabled] <b>[Enabled]</b>	PS4 Enable/Disable. 0 - Disabled, 1 - Enabled. Uses BIOS VR mailbox command 0x3
IMON Slope	<b>minimum = 0</b> <b>maximum = 200</b> <b>step = 1</b> <b>default = 0</b>	IMON Slope defined in 1/100 increments. Range is 0-200. For a 1.25 slope, enter 125. 0 = AUTO. Uses BIOS VR mailbox command 0x4.
IMON Offset	<b>minimum = 0</b> <b>maximum = 63999</b> <b>step = 1</b> <b>default = 0</b>	IMON Offset defined in 1/1000 increments. Range is 0-63999. For an offset of 25.348, enter 25348. IMON Uses BIOS VR mailbox command 0x4.
IMON Prefix	<b>[+]</b> <b>[-]</b>	Sets the offset value as positive or negative.
VR Current Limit	<b>minimum = 0</b> <b>maximum = 2048</b> <b>step = 1</b> <b>default = 0</b>	Voltage Regulator Current Limit (Icc Max). This value represents the Maximum instantaneous current allowed at any given time. The value is represented in 1/4 A increments. A value of 400 = 100A. 0 means AUTO. Uses BIOS VR mailbox command 0x6.
VR Voltage Limit	<b>minimum = 0</b> <b>maximum = 7999</b> <b>step = 1</b> <b>default = 0</b>	VR Voltage Limit, defined in mV. Range is 0-7999mV. For a Voltage Limit of 1.25V, enter 1250. 0 = AUTO. Uses BIOS VR mailbox command 0x6
TDC Enable	<b>[Disabled]</b> [Enabled]	TDC Enable. 0- Disable, 1 - Enable
TDC Current Limit	<b>minimum = 0</b> <b>maximum = 32767</b> <b>step = 125</b> <b>default = 0</b>	TDC Current Limit, defined in 1/8A increments. Range 0-32767. For a TDC Current Limit of 125A, enter 1000. 0 = 0 Amps. Uses BIOS VR mailbox command 0x1A.
TDC Time Window	<b>[1 ms]</b> [2 ms] [3 ms] [4 ms] [5 ms] [6 ms] [7 ms] [8ms] [10ms]	TDC Time Window, value in milliseconds. 1ms is default. Range from 1ms to 10ms, except for 9ms. 9ms has no valid encoding in the MSR definition.
TDC Lock	<b>[Disabled]</b> [Enabled]	TDC Lock

### 2.2.12.1.3.5 RFI Settings

**Table 2-2-12-1-3-5. RFI Settings**

BIOS Setting	Options	Description
RFI Domain		
RFI Current Frequency	No Options	RFI Current Frequency (Show as <i>SETUP_CPU_FEATURES.FivrSupported</i> is not 0)
RFI Frequency	<b>minimum = 0</b> <b>maximum = 1918</b> <b>default = 0</b>	Set desired RFI frequency, in increments of 100KHz. (For a frequency of 100.6MHz, enter 1006.) (Show as <i>SETUP_CPU_FEATURES.FivrSupported</i> is not 0)
FIVR Spread Spectrum	[Disabled] <b>[Enable]</b>	Enable or Disable the FIVR Spread Spectrum (Show as <i>SETUP_CPU_FEATURES.FivrSupported</i> is not 0)
RFI Spread Spectrum	[0.5%] [1%] <b>[1.5%]</b> [2%] [3%] [4%] [5%] [6%]	Set the Spread Spectrum (Show as <i>SETUP_CPU_FEATURES.McivrSupported</i> is not 0)

### 2.2.12.1.4 Custom P-state Table

**Table 2-2-12-1-4. Custom P-state Table**

BIOS Setting	Options	Description
Custom P-state Table		
Number of P states	<b>minimum = 0</b> <b>maximum = MAX_CUSTOM_P_STATES</b> <b>step = 0</b> <b>default 0</b> <b>(MAX_CUSTOM_P_STATES = 40)</b>	Sets the number of custom P-states. At least 2 states must be present.

### 2.2.12.1.5 Power Limit 3 Settings

**Table 2-2-12-1-5. Power Limit 3 Settings**

BIOS Setting	Options	Description
Power Limit 3 Override	<b>[Disabled]</b> [Enabled]	Enable/Disable Power Limit 3 override. If this option is disabled, BIOS will leave the hardware default values for Power Limit 3 and Power Limit 3 Time Window. (Below options will show at this option set Enabled)

Power Limit 3	<b>minimum = 0</b> <b>maximum = 4095875</b> <b>step = 125</b> <b>default = 0</b>	Power Limit 3 in Milli Watts. BIOS will round to the nearest 1/8W when programming. For 12.50W, enter 12500. XE SKU: Any value can be programmed. Overclocking SKU: Value must be between Max and Min Power Limits (specified by PACKAGE_POWER_SKU_MSR). Other SKUs: This value must be between Min Power Limit and TDP Limit. If the value is 0, BIOS leaves the hardware default value
Power Limit 3 Time Window	<b>[0]</b> [3] [4] [5] [6] [7] [8] [10] [12] [14] [16] [20] [24] [28] [32] [40] [48] [56] [64]	Power Limit 3 Time Window value in Milli seconds. The value may vary from 3 to 64(max).Indicates the time window over which Power Limit 3 value should be maintained. If the value is 0, BIOS leaves the hardware default value
Power Limit 3 Duty Cycle	<b>minimum = 0</b> <b>maximum = 100</b> <b>default = 0</b>	Specify the duty cycle in percentage that the CPU is required to maintain over the configured time window. Range is 0-100.
Power Limit 3 Lock	<b>[Disabled]</b> [Enabled]	Power Limit 3 MSR 615h Lock. When enabled PL3 configurations are locked during OS. When disabled PL3 configuration can be changed during OS.

### 2.2.12.1.6 CPU Lock Configuration

**Table 2-2-12-1-6. CPU Lock Configuration**

BIOS Setting	Options	Description
CFG Lock	[Disabled] <b>[Enabled]</b>	Configure MSR 0xE2[15], CFG Lock bit
Overclocking Lock	[Disabled] <b>[Enabled]</b>	Enable/Disable Overclocking Lock (BIT 20) in FLEX_RATIO(194) MSR

### 2.2.12.2 GT - Power Management Control

**Table 2-2-12-2. GT - Power Management Control**

BIOS Setting	Options	Description
GT - Power Management Control		
RC6(Render Standby)	[Disabled] <b>[Enabled]</b>	Check to enable render standby support. (This options can be set at PM Support set Enabled)

Maximum GT frequency	<b>[Default Max Frequency]</b> [100Mhz] [150Mhz] [200Mhz] [250Mhz] [300Mhz] [350Mhz] [400Mhz] [450Mhz] [500Mhz] [550Mhz] [600Mhz] [650Mhz] [700Mhz] [750Mhz] [800Mhz] [850Mhz] [900Mhz] [950Mhz] [1000Mhz] [1050Mhz] [1100Mhz] [1150Mhz] [1200Mhz]	Maximum GT frequency limited by the user. Choose between 100MHz (RPN) and 1000MHz (RP0). Value beyond the range will be clipped to min/max supported by SKU <u>(Below options can be set at this option set Default Max Frequency)</u>
Disable Turbo GT frequency	[Enabled] <b>[Disabled]</b>	Enabled: Disables Turbo GT frequency. Disabled: GT frequency is not limited

### 2.2.13 OverClocking Performance Menu

**Table 2-2-13. OverClocking Performance Menu**

BIOS Setting	Options	Description
OverClocking Performance Menu		(Show as <code>SETUP_VOLATILE_DATA.PlatformType</code> is not <code>TypeUltUlx</code> )
OverClocking Feature	<b>[Disabled]</b> [Enabled]	Performance Menu for Processor and Memory. (Show as <u><i>SystemConfig.OverClockingSupport</i></u> is not 0)
WDT Enable	<b>[Disabled]</b> [Enabled]	Enable/Disable WatchDog Timer. Note: This option is ignored on debug BIOS.
<u>(Below options will show at OverClocking Feature set Enabled)</u>		
BCLK Frequency	100.00 MHz	None (Show as <u><i>SETUP_VOLATILE_DATA.PlatformType</i></u> is not <code>TypeTrad</code> )
Processor	(See Section 2.2.13.1)	Processor Bus Ratio Override and Bus Speed Override.
Ring	(See Section 2.2.13.2)	Ring Ratio and Voltage Settings
GT	(See Section 2.2.13.3)	GT Ratio Override and Delta voltage programming
Uncore	(See Section 2.2.13.4)	Uncore Overclocking Menu
Voltage PLL Trim Controls	(See Section 2.2.13.5)	Voltage PLL Trim Controls Menu
Platform Voltage Overrides	(See Section 2.2.13.6)	Platform Voltages related Overclocking Menu
Memory	(See Section 2.2.13.7)	Memory Overclocking Menu

## 2.2.13.1 Processor

**Table 2-2-13-1. Processor**

BIOS Setting	Options	Description
Processor		
Core Max OC Ratio	<b>minimum = 0</b> <b>maximum = 120</b> <b>step = 1</b> <b>default = 0</b>	Sets the maximum OC Ratio for the CPU Core. Uses Mailbox MSR 0x150, cmd 0x10, 0x11. Range 0-255.
Core Voltage Mode	<b>[Adaptive]</b> [Override]	Selects between Adaptive and Override Voltage modes. In Override Mode the voltage selected will be applied over all operating frequencies. In Adaptive Mode the voltage is interpolated only in turbo mode. Uses Mailbox MSR 0x150, cmd 0x10, 0x11.
Core Voltage Override	<b>minimum = 0</b> <b>maximum = 2000</b> <b>step = 1</b> <b>default = 0</b>	Specifies the Override Voltage applied to the IA Core domain. This voltage is specified in millivolts. Uses Mailbox MSR 0x150, cmd 0x11. Range 0-2000 mV. <u>(This option will show at Core Voltage Mode set [Override])</u>
Core Extra Turbo Voltage	<b>minimum = 0</b> <b>maximum = 2000</b> <b>step = 1</b> <b>default = 0</b>	Specifies the extra turbo voltage applied while IA Core is operating in turbo mode. Uses Mailbox MSR 0x150, cmd 0x10, 0x11. Range 0-2000 mV. <u>(This option will show at Core Voltage Mode set [Adaptive])</u>
Core Voltage Offset	<b>minimum = 0</b> <b>maximum = 1000</b> <b>step = 1</b> <b>default = 0</b>	Specifies the Offset Voltage applied to the IA Core domain. This voltage is specified in millivolts. Uses Mailbox MSR 0x150, cmd 0x11. Range -500 to 500 mV
Offset Prefix	<b>[+]</b> [-]	Sets the offset value as positive or negative.
AVX2 Ratio Offset	<b>minimum = 0</b> <b>maximum = 31</b> <b>step = 1</b> <b>default = 0</b>	AVX2 Ratio Offset. Specifies number of bins to decrease AVX ratio vs. Core Ratio. AVX is a more stressful workload, it is helpful to lower the AVX ratio to ensure maximum possible ratio for SSE workloads. Uses Mailbox MSR 0x150, cmd 0x1B. Range 0 - 31. 0 = No offset.
TjMax Offset	<b>minimum = 0</b> <b>maximum = 63</b> <b>step = 1</b>	TjMax Offset. Specified value here is clipped by pCode (125 - TjMax Offset) to support TjMax in the

	<b>default = 0</b>	range of 62 to 115 deg Celsius. Uses Mailbox MSR 0x37, command 0x01. Range 10 - 63. 0 = No offset. Only valid on CFL-S 8+2.
Thermal Velocity Boost (TVB)		
TVB Ratio Clipping	<b>[Disabled]</b> [Enabled]	This service controls Core frequency reduction caused by high package temperatures for processors that implement the Intel Thermal Velocity Boost (TVB) feature. It is required to be disabled for supporting overclocking at frequencies higher than the default max turbo frequency. Uses Overclocking Mailbox command 0x18/0x19.
TVB Voltage Optimizations	[Disabled] <b>[Enabled]</b>	This service controls thermal based voltage optimizations for processors that implement the Intel Thermal Velocity Boost (TVB) feature. Uses Overclocking Mailbox command 0x18/0x19.

### 2.2.13.2 Ring

**Table 2-2-13-2. Ring**

BIOS Setting	Options	Description
Ring		
Ring Max OC Ratio	<b>minimum = 0</b> <b>maximum = 255</b> <b>step = 1</b> <b>default = 0</b>	Sets the maximum OC Ratio for the CPU Ring. Uses Mailbox MSR 0x150, cmd 0x10, 0x11. Range 0-255.
Ring Voltage Mode	<b>[Adaptive]</b> [Override]	Selects between Adaptive and Override Voltage modes. In Override Mode the voltage selected will be applied over all operating frequencies. In Adaptive Mode the voltage is interpolated only in turbo mode. Uses Mailbox MSR 0x150, cmd 0x10, 0x11.
Ring Voltage Override	<b>minimum = 0</b> <b>maximum = 2000</b> <b>step = 1</b> <b>default = 0</b>	Specifies the Override Voltage applied to the Ring domain. This voltage is specified in millivolts. Uses Mailbox MSR 0x150, cmd 0x11. Range 0-2000 mV. (Show as <i>CPU_CFL</i> is not defined, <i>CPU_SETUP.RingVoltageMode</i> is not [Adaptive])

Ring Extra Turbo Voltage	<b>minimum = 0</b> <b>maximum = 2000</b> <b>step = 1</b> <b>default = 0</b>	Specifies the extra turbo voltage applied while ring is operating in turbo mode. Uses Mailbox MSR 0x150, cmd 0x10, 0x11. Range 0-2000 mV. (Show as <u>CPU_CFL</u> is not defined, CPU_SETUP.RingVoltageMode is not [Override])
Ring Voltage Offset	<b>minimum = 0</b> <b>maximum = 1000</b> <b>step = 1</b> <b>default = 0</b>	Specifies the Offset Voltage applied to the Ring domain. This voltage is specified in millivolts. Uses Mailbox MSR 0x150, cmd 0x11. Range -500 to 500 mV (Show as <u>CPU_CFL</u> is not defined)
Offset Prefix	[+] [-]	Sets the offset value as positive or negative. (Show as <u>CPU_CFL</u> is not defined)
Ring Down Bin	[Disabled] [Enabled] 2.2.14.1.1	Enable/Disable Ring Downbin feature. Enabled - CPU will down bin the ring ratio, which means the requested max ring ratio will not be observed. Disable - CPU will not down bin the ring ratio and the requested ring ratio limit will be observed. Default for Overclocking is "Disabled" to allow for a predictable ring ratio. Uses OC mailbox command 0x19.
Min Ring Ratio Limit	<b>minimum = 0</b> <b>maximum = 83</b> <b>step = 1</b> <b>default = 0</b>	This sets the minimum ring ratio limit. 0 - Auto/HW default. 1-LFM are invalid ratio settings.
Max Ring Ratio Limit	<b>minimum = 0</b> <b>maximum = 83</b> <b>step = 1</b> <b>default = 0</b>	This sets the maximum ring ratio limit. 0 - Auto/HW default. 1-LFM are invalid ratio settings.

### 2.2.13.3 GT

**Table 2-2-13-3. GT**

BIOS Setting	Options	Description
GT Domain		
GT OverClocking Frequency	<b>minimum = 0</b> <b>maximum = 255</b> <b>step = 1</b> <b>default = 0</b>	Overclocked RP0 Frequency (MLC Clk) in multiples of 50 MHz. Range 0-255.
GT Voltage Mode	[Adaptive] [Override]	Selects between Adaptive and Override Voltage modes. In Override Mode the voltage selected

		will be applied over all operating frequencies. In Adaptive Mode the voltage is interpolated only in turbo mode. Uses Mailbox MSR 0x150, cmd 0x10, 0x11.
GT Voltage Override	<b>minimum = 0</b> <b>maximum = 2000</b> <b>step = 1</b> <b>default = 0</b>	Specifies the Override Voltage applied to the GT domain. This voltage is specified in millivolts. Uses Mailbox MSR 0x150, cmd 0x11. Range 0-2000 mV. <u>(This option will show at GT Voltage Mode set [Override])</u>
GT Extra Turbo Voltage	<b>minimum = 0</b> <b>maximum = 2000</b> <b>step = 1</b> <b>default = 0</b>	Specifies the extra turbo voltage applied while GT is operating in turbo mode. Unit is in millivolts. Uses Mailbox MSR 0x150, cmd 0x11. Range 0-2000 mV. <u>(This option will show at GT Voltage Mode set [Adaptive])</u>
GT Voltage Offset	<b>minimum = 0</b> <b>maximum = 1000</b> <b>step = 1</b> <b>default = 0</b>	Specifies the Offset Voltage applied to the GT domain. This voltage is specified in millivolts. Uses Mailbox MSR 0x150, cmd 0x11. Range -1000 to 1000 mV.
Offset Prefix	[+] [-]	Sets the offset value as positive or negative.
GT Unslice Domain		
GT OverClocking Frequency	<b>minimum = 0</b> <b>maximum = 60</b> <b>step = 1</b> <b>default = 0</b>	Overclocked RP0 Frequency (MLC Clk) in multiples of 50 MHz. Range 0-255.
GT Voltage Mode	[Adaptive] [Override]	Selects between Adaptive and Override Voltage modes. In Override Mode the voltage selected will be applied over all operating frequencies. In Adaptive Mode the voltage is interpolated only in turbo mode. Uses Mailbox MSR 0x150, cmd 0x10, 0x11.
GT Voltage Override	<b>minimum = 0</b> <b>maximum = 2000</b> <b>step = 1</b> <b>default = 0</b>	Specifies the Override Voltage applied to the GT domain. This voltage is specified in millivolts. Uses Mailbox MSR 0x150, cmd 0x11. Range 0-2000 mV. <u>(This option will show at GT Voltage Mode set [Override])</u>
GT Extra Turbo Voltage	<b>minimum = 0</b> <b>maximum = 2000</b> <b>step = 1</b> <b>default = 0</b>	Specifies the extra turbo voltage applied while GT is operating in turbo mode. Unit is in millivolts.

		Uses Mailbox MSR 0x150, cmd 0x11. Range 0-2000 mV. <u>(This option will show at GT Voltage Mode set [Adaptive])</u>
GTU Voltage Offset	<b>minimum = 0</b> <b>maximum = 1000</b> <b>step = 1</b> <b>default = 0</b>	Specifies the Offset Voltage applied to the GT domain. This voltage is specified in millivolts. Uses Mailbox MSR 0x150, cmd 0x11. Range -1000 to 1000 mV.
Offset Prefix	[+] [-]	Sets the offset value as positive or negative.

### 2.2.13.4 Uncore

**Table 2-2-13-4. Uncore**

BIOS Setting	Options	Description
Uncore		
Uncore Voltage Offset	<b>minimum = 0</b> <b>maximum = 1000</b> <b>step = 1</b> <b>default = 0</b>	Specifies the Offset Voltage applied to the Uncore domain. This voltage is specified in millivolts. Uses Mailbox MSR 0x150, cmd 0x11. Range -1000 to 1000 mV
Offset Prefix	[+] [-]	Sets the offset value as positive or negative.

### 2.2.13.5 Voltage PLL Trim Controls

**Table 2-2-13-5. Voltage PLL Trim Controls**

BIOS Setting	Options	Description
Voltage PLL Trim Controls		
Core PLL Voltage Offset	<b>minimum = 0</b> <b>maximum = 63</b> <b>step = 1</b> <b>default = 0</b>	PLL Voltage Offset, Range 0-63. Units are in 17.5mV. This control can be used to increase the range of this domain frequency in extreme overclocking conditions.
GT PLL Voltage Offset	<b>minimum = 0</b> <b>maximum = 63</b> <b>step = 1</b> <b>default = 0</b>	PLL Voltage Offset, Range 0-63. Units are in 17.5mV. This control can be used to increase the range of this domain frequency in extreme overclocking conditions.
Ring PLL Voltage Offset	<b>minimum = 0</b> <b>maximum = 63</b> <b>step = 1</b> <b>default = 0</b>	PLL Voltage Offset, Range 0-63. Units are in 17.5mV. This control can be used to increase the range of this domain frequency in extreme overclocking conditions.

System Agent PLL Voltage Offset	<b>minimum = 0</b> <b>maximum = 63</b> <b>step = 1</b> <b>default = 0</b>	PLL Voltage Offset, Range 0-63. Units are in 17.5mV. This control can be used to increase the range of this domain frequency in extreme overclocking conditions.
Memory Controller PLL Voltage Offset	<b>minimum = 0</b> <b>maximum = 63</b> <b>step = 1</b> <b>default = 0</b>	PLL Voltage Offset, Range 0-63. Units are in 17.5mV. This control can be used to increase the range of this domain frequency in extreme overclocking conditions.

### 2.2.13.6 Platform Voltage Overrides

**Table 2-2-13-6. Platform Voltage Overrides**

BIOS Setting	Options	Description
Platform Voltage Overrides		
VccCore Override Enable	<b>[Disabled]</b> [Enabled]	Overrides the VccCore voltage using SMBUS/PMBUS interface of VRM. Use the next option for exact voltage configuration
VccCore	<b>minimum = 800</b> <b>maximum = 2550</b> <b>step = 10</b> <b>default = 1300</b>	Range of VccCore voltage - Up to 2550 mV. (This option will show at VccCore Override Enable set [Enabled])
VccST Override Enable	<b>[Disabled]</b> [Enabled]	Overrides the VccST voltage using SMBUS/PMBUS interface of VRM. Use the next option for exact voltage configuration
VccST	<b>minimum = 250</b> <b>maximum = 1500</b> <b>step = 10</b> <b>default = 1020</b>	Range of VccST voltage - 250 mV to 1500 mV. (This option will show at VccST Override Enable set [Enabled])
VccSA Override Enable	<b>[Disabled]</b> [Enabled]	Overrides the VccSA voltage using SMBUS/PMBUS interface of VRM. Use the next option for exact voltage configuration
VccSA	<b>minimum = 250</b> <b>maximum = 1520</b> <b>step = 10</b> <b>default = 1050</b>	Range of VccSA voltage - Up to 1500 mV. (This option will show at VccSA Override Enable set [Enabled])
VccSFR_OC Override Enable	<b>[Disabled]</b> [Enabled]	Overrides the VccSFR_OC voltage using SMBUS/PMBUS interface of VRM. Use the next option for exact voltage configuration
VccSFR_OC	<b>minimum = 1000</b> <b>maximum = 2520</b> <b>step = 10</b> <b>default = 1250</b>	Range of VccSFR_OC voltage range - 1000mV to 2520mV.

		(This option will show at <u>VccSFR_OC Override Enable set [Enabled]</u> )
VccSFR Override Enable	<b>[Disabled]</b> [Enabled]	Overrides the VccSFR voltage using SMBUS/PMBUS interface of VRM. Use the next option for exact voltage configuration
VccSFR	<b>minimum = 690</b> <b>maximum = 2050</b> <b>step = 10</b> <b>default = 1020</b>	Range of VccSFR voltage - 690mV to 2050mV. (This option will show at <u>VccSFR Override Enable set [Enabled]</u> )
VccIO Override Enable	<b>[Disabled]</b> [Enabled]	Overrides the VccIO voltage using SMBUS/PMBUS interface of VRM. Use the next option for exact voltage configuration
VccIO	<b>minimum = 900</b> <b>maximum = 1520</b> <b>step = 5</b> <b>default = 950</b>	Range of VccIO voltage - 900 mV to 1520 mV. (This option will show at <u>VccIO Override Enable set [Enabled]</u> )
Core VR Loadline Override	<b>[Disabled]</b> [Enabled]	Overrides the Core VR DC Loadline. Use the next option for exact voltage configuration
DC Loadline value	[-100 uOhm] [0 uOhm] [100 uOhm] [700 uOhm] [900 uOhm] [1000 uOhm] [1200 uOhm] [1300 uOhm] [1400 uOhm] [1500 uOhm] [1700 uOhm] [1800 uOhm] <b>[2100 uOhm]</b>	DC Loadline value as 2100 then override matches to 0xC produces the same value as without override (2.1mOhm). (This option will show at <u>Core VR Loadline Override set [Enabled]</u> )

### 2.2.13.7 Memory

**Table 2-2-13-7. Memory**

BIOS Setting	Options	Description
Memory Profile: Default Custom XMP1 XMP2		
tCK [MHz]	0000000 0000000 0000000 0000000	
tCL	00000 00000 00000 00000	
tRCD/tRP	00000 00000 00000 00000	
tRAS	00000 00000 00000 00000	
tCWL	00000 00000 00000 00000	
tFAW	00000 00000 00000 00000	
tREFI	00000 00000 00000 00000	

	tRFC 00000 00000 00000 00000	
	tRRD 00000 00000 00000 00000	
	tRRD_L 00000 00000 00000 00000	
	tRRD_S 00000 00000 00000 00000	
	TRTP 00000 00000 00000 00000	
	TWR 00000 00000 00000 00000	
	TWTR 00000 00000 00000 00000	
	tWTR_L 00000 00000 00000 00000	
	tWTR_S 00000 00000 00000 00000	
	Nmode 00000 00000 00000 00000	
	VDD [mV] 00000 00000 00000 00000	
Realtime Memory Timing	<b>[Disabled]</b> [Enabled]	Enable/Disable realtime memory timings. When enabled, the system will allow performing realtime memory timing changes after MRC_DONE.
Memory profile	<b>[Default profile]</b> [Custom profile]	Select DIMM timing profile. The below values start with the currently running values and don't auto populate.
Turn Around Timing	(See Section 2.2.12.7.1)	Knobs to override default timings. 0 is no override.
Memory Reference Clock	<b>[133]</b> [100]	100MHz, 133MHz.
Memory Ratio	CPU_CFL is defined: <b>[Auto]</b> [3] [4] [5] [6] [7] [8] [9] [10] [11] [12] [13][14] [15] [16] [17] [18] [19][20] [21] [22] [23] [24] [25][26] [27] [28] [29] [30] [31]  else: <b>[Auto]</b> [3] [4] [5] [6] [7] [8] [9] [10] [11] [12] [13][14] [15]	Automatic or the frequency will equal ratio times reference clock. Set to Auto to recalculate memory timings listed below.
QCLK Odd Ratio	<b>[Disabled]</b> [Enabled]	Adds 133 or 100 MHz to QCLK frequency, depending on RefClk
tCL	<b>minimum = 0</b> <b>maximum = 36</b> <b>step = 1</b> <b>default = 0</b>	CAS Latency, 0: AUTO, max: 31

tRCD/tRP	<b>minimum = 0</b> <b>maximum = 63</b> <b>step = 1</b> <b>default = 0</b>	RAS to CAS delay time and Row Precharge delay time, 0: AUTO, max: 63
tRAS	<b>minimum = 0</b> <b>maximum = 90</b> <b>step = 1</b> <b>default = 0</b>	RAS Active Time, 0: AUTO, max: 64
tCWL	<b>minimum = 0</b> <b>maximum = 34</b> <b>step = 1</b> <b>default = 0</b>	Min CAS Write Latency Delay Time, 0: AUTO, max: 20
tFAW	<b>minimum = 0</b> <b>maximum = 127</b> <b>step = 1</b> <b>default = 0</b>	Min Four Activate Window Delay Time, 0: AUTO, max: 63
tREFI	<b>minimum = 0</b> <b>maximum = 65535</b> <b>step = 1</b> <b>default = 0</b>	Refresh Interval, 0: AUTO, max: 65535
tRFC	<b>minimum = 0</b> <b>maximum = 1023</b> <b>step = 1</b> <b>default = 0</b>	Min Refresh Recovery Delay Time, 0: AUTO, max: 1023
tRRD	<b>minimum = 0</b> <b>maximum = 31</b> <b>step = 1</b> <b>default = 0</b>	Min Row Active to Row Active Delay Time, 0: AUTO, max: 31
tRRD_L	<b>minimum = 0</b> <b>maximum = 31</b> <b>step = 1</b> <b>default = 0</b>	Min Row Active to Row Active Delay Time for Same Bank Group, 0: AUTO, max: 31 (Show as <u>CPU_CFL</u> is defined)
tRRD_S	<b>minimum = 0</b> <b>maximum = 31</b> <b>step = 1</b> <b>default = 0</b>	Min Row Active to Row Active Delay Time for Different Bank Group, 0: AUTO, max: 31 (Show as <u>CPU_CFL</u> is defined)
tRTP	<b>minimum = 0</b> <b>maximum = 16</b> <b>step = 1</b> <b>default = 0</b>	Min Internal Read to Precharge Command Delay Time, 0: AUTO, max: 15. DDR4 legal values: 5, 6, 7, 8, 9, 10, 12
tWR	<b>[Auto]</b> [5] [6] [7] [8] [10] [12] [14] [16] [18] [20] [22] [24] [28] [30] [32] [34] [38] [40] [44]	Min Write Recovery Time, 0: AUTO, legal values: 5, 6, 7, 8, 10, 12, 14, 16, 18, 20, 24
tWTR	<b>minimum = 0</b> <b>maximum = 28</b> <b>step = 1</b> <b>default = 0</b>	Min Internal Write to Read Command Delay Time, 0: AUTO, max: 28

tWTR_L	<b>minimum = 0</b> <b>maximum = 60</b> <b>step = 1</b> <b>default = 0</b>	Min Internal Write to Read Command Delay Time for Same Bank Group, 0: AUTO, max: 60 (Show as <u>CPU_CFL</u> is defined)
tWTR_S	<b>minimum = 0</b> <b>maximum = 28</b> <b>step = 1</b> <b>default = 0</b>	Min Internal Write to Read Command Delay Time for Different Bank Group, 0: AUTO, max: 28 (Show as <u>CPU_CFL</u> is defined)
Memory Voltage	<b>[Default]</b> [0.60 Volts] [1.10 Volts] [1.15 Volts] [1.20 Volts] [1.25 Volts] [1.30 Volts] [1.35 Volts] [1.40 Volts] [1.45 Volts] [1.50 Volts] [1.55 Volts] [1.60 Volts] [1.65 Volts]	Memory Voltage Override (Vddq). Default = no override
NMode	<b>minimum = 0</b> <b>maximum = 2</b> <b>step = 1</b> <b>default = 0</b>	System command rate, range 0-2, 0 means AUTO, 1 = 1N, 2 = 2N
Command Rate Support	[Disabled] [1 CMD] [2 CMD] <b>[3 CMD]</b> [4 CMD] [5 CMD] [6 CMD] [7 CMD]	CMD Rate and Limit Support Option. NOTE: ONLY supported in 1N Mode (Show as <u>SA_SETUP.NmodeSupport</u> is 1)
DllBwEn[0]	<b>minimum = 0</b> <b>maximum = 7</b> <b>step = 1</b> <b>default = 0</b>	DllBwEn[0], for 1067 (0..7)
DllBwEn[1]	<b>minimum = 0</b> <b>maximum = 7</b> <b>step = 1</b> <b>default = 1</b>	DllBwEn[1], for 1333 (0..7)
DllBwEn[2]	<b>minimum = 0</b> <b>maximum = 7</b> <b>step = 1</b> <b>default = 2</b>	DllBwEn[2], for 1600 (0..7)
DllBwEn[3]	<b>minimum = 0</b> <b>maximum = 7</b> <b>step = 1</b> <b>default = 2</b>	DllBwEn[3], for 1867 and up (0..7)
VDD	N/A	

### 2.2.13.7.1 Turn Around Timing

**Table 2-2-13-7-1. Turn Around Timing**

BIOS Setting	Options	Description
Current Turn Around Times	SG DG DR DD	

Channel 0		(Show as SETUP_VOLATILE_DATA.DimmPresent[OFFSET_0] is not 0 AND SETUP_VOLATILE_DATA.DimmPresent[OFFSET_1] is not 0)
Read-to-Read	00000 00000 00000 00000	
Read-to-Write	00000 00000 00000 00000	
Write-to-Read	00000 00000 00000 00000	
Write-to-Write	00000 00000 00000 00000	
Channel 1		(Show as SETUP_VOLATILE_DATA.DimmPresent[OFFSET_2] is not 0 AND SETUP_VOLATILE_DATA.DimmPresent[OFFSET_3] is not 0)
Read-to-Read	00000 00000 00000 00000	
Read-to-Write	00000 00000 00000 00000	
Write-to-Read	00000 00000 00000 00000	
Write-to-Write	00000 00000 00000 00000	
tRd2RdSG	<b>minimum = 0</b> <b>maximum = 54</b> <b>step = 1</b> <b>default = 0</b>	Delay between Read-to-Read commands in the same Bank Group. 0-Auto, Range 4-54.
tRd2RdDG	<b>minimum = 0</b> <b>maximum = 54</b> <b>step = 1</b> <b>default = 0</b>	Delay between Read-to-Read commands in different Bank Group for DDR4. All other DDR technologies should set this equal to SG. 0-Auto, Range 4-54.
tRd2RdDR	<b>minimum = 0</b> <b>maximum = 54</b> <b>step = 1</b> <b>default = 0</b>	Delay between Read-to-Read commands in different Ranks. 0-Auto, Range 4-54.
tRd2RdDD	<b>minimum = 0</b> <b>maximum = 54</b> <b>step = 1</b> <b>default = 0</b>	Delay between Read-to-Read commands in different DIMMs. 0-Auto, Range 4-54.
tRd2WrSG	<b>minimum = 0</b> <b>maximum = 54</b> <b>step = 1</b> <b>default = 0</b>	Delay between Read-to-Write commands in the same Bank Group. 0-Auto, Range 4-54.
tRd2WrDG	<b>minimum = 0</b> <b>maximum = 54</b> <b>step = 1</b> <b>default = 0</b>	Delay between Read-to-Write commands in different Bank Group for DDR4. All other DDR technologies should set this equal to SG. 0-Auto, Range 4-54.
tRd2WrDR	<b>minimum = 0</b> <b>maximum = 54</b> <b>step = 1</b> <b>default = 0</b>	Delay between Read-to-Write commands in different Ranks. 0-Auto, Range 4-54.
tRd2WrDD	<b>minimum = 0</b> <b>maximum = 54</b> <b>step = 1</b>	Delay between Read-to-Write commands in different DIMMs. 0-Auto, Range 4-54.

	<b>default = 0</b>	
tWr2RdSG	<b>minimum = 0 maximum = 86 step = 1 default = 0</b>	Delay between Write-to-Read commands in the same Bank Group. 0-Auto, Range 4-86.
tWr2RdDG	<b>minimum = 0 maximum = 54 step = 1 default = 0</b>	Delay between Write-to-Read commands in different Bank Group for DDR4. All other DDR technologies should set this equal to SG. 0-Auto, Range 4-54.
tWr2RdDR	<b>minimum = 0 maximum = 54 step = 1 default = 0</b>	Delay between Write-to-Read commands in different Ranks. 0-Auto, Range 4-54.
tWr2RdDD	<b>minimum = 0 maximum = 54 step = 1 default = 0</b>	Delay between Write-to-Read commands in different DIMMs. 0-Auto, Range 4-54.
tWr2WrSG	<b>minimum = 0 maximum = 54 step = 1 default = 0</b>	Delay between Write-to-Write commands in the same Bank Group. 0-Auto, Range 4-54.
tWr2WrDG	<b>minimum = 0 maximum = 54 step = 1 default = 0</b>	Delay between Write-to-Write commands in different Bank Group for DDR4. All other DDR technologies should set this equal to SG. 0-Auto, Range 4-54.
tWr2WrDR	<b>minimum = 0 maximum = 54 step = 1 default = 0</b>	Delay between Write-to-Write commands in different Ranks. 0-Auto, Range 4-54.
tWr2WrDD	<b>minimum = 0 maximum = 54 step = 1 default = 0</b>	Delay between Write-to-Write commands in different DIMMs. 0-Auto, Range 4-54.

## 2.2.14 Memory Configuration

**Table 2-2-14. Memory Configuration**

BIOS Setting	Options	Description
Memory Thermal Configuration	(See Section 2.2.14.1)	Memory Thermal Configuration Options
Memory Training Algorithms	(See Section 2.2.14.2)	Enable/Disable Memory Training Algorithms
Memory	(See Section 2.2.14.3)	Memory Overclocking Menu.
Memory Configuration		
Memory RC Version	No options	Memory RC Version

Memory Frequency	No options	Displays the Frequency of Memory
Memory Timings (tCL-tRCD-tRP-tRAS)	No options	Memory Timings
Controller 0 Channel 0 Slot 0	No options	Controller Channel Slot Subtitle
Size	No options	Memory Size in the Slot.
Number of Ranks	No options	Number of Ranks in the slot
Manufacturer	No options	DIMM / DRAM Manufacturer Value
Controller 0 Channel 1 Slot 0	No options	Controller Channel Slot Subtitle
Size	No options	Memory Size in the Slot.
Number of Ranks	No options	Number of Ranks in the slot
Manufacturer	No options	DIMM / DRAM Manufacturer Value
Controller 0 Channel 2 Slot 0	No options	Controller Channel Slot Subtitle
Size	No options	Memory Size in the Slot.
Number of Ranks	No options	Number of Ranks in the slot
Manufacturer	No options	DIMM / DRAM Manufacturer Value
Controller 0 Channel 3 Slot 0	No options	Controller Channel Slot Subtitle
Size	No options	Memory Size in the Slot.
Number of Ranks	No options	Number of Ranks in the slot
Manufacturer	No options	DIMM / DRAM Manufacturer Value
Controller 1 Channel 0 Slot 0	No options	Controller Channel Slot Subtitle
Size	No options	Memory Size in the Slot.
Number of Ranks	No options	Number of Ranks in the slot
Manufacturer	No options	DIMM / DRAM Manufacturer Value
Controller 1 Channel 1 Slot 0	No options	Controller Channel Slot Subtitle
Size	No options	Memory Size in the Slot.
Number of Ranks	No options	Number of Ranks in the slot

	Manufacturer	No options	DIMM / DRAM Manufacturer Value
Controller 1 Channel 2 Slot 0		No options	Controller Channel Slot Subtitle
	Size	No options	Memory Size in the Slot.
	Number of Ranks	No options	Number of Ranks in the slot
	Manufacturer	No options	DIMM / DRAM Manufacturer Value
Controller 1 Channel 3 Slot 0		No options	Controller Channel Slot Subtitle
	Size	No options	Memory Size in the Slot.
	Number of Ranks	No options	Number of Ranks in the slot
	Manufacturer	No options	DIMM / DRAM Manufacturer Value
Debug Value		<b>minimum = 0</b> <b>maximum = 0xFFFFFFFF</b> <b>step = 1</b> <b>default = 0</b>	Debug Value
MRC ULT Safe Config		<b>[Disabled]</b> [Enabled]	MRC ULT Safe Config for PO
LPDDR DqDqs Re-Training		[Disabled] <b>[Enabled]</b>	Disable/Enable LPDDR DqDqs Re Training
Safe Mode Support		<b>[Disabled]</b> [Enabled]	Safe Mode enable support. Option will be used for changes/WAs that may affect an stable MRC
Memory Test on Warm Boot		[Disabled] <b>[Enabled]</b>	Enable Or Disable Base Memory Test Run on Warm Boot
Maximum Memory Frequency		CPU_CFL is defined: [Auto] [1067] [1200] [1333] [1400] [1600] [1800] [1867] [2000] <b>[2133]</b> [2200] [2400] [2600] [2667] [2800] [2933] [3000] [3200] [3400] [3467] [3600] [3733] [3800] [4000] [4200] [4267] [4400] [4533] [4600] [4800] [5000] [5067] [5200] [5333] [5400] [5600] [5800] [5867] [6000] [6133][6200]  else: <b>[Auto]</b> [1067] [1200] [1333] [1400] [1600] [1800] [1867] [2000] [2133] [2200] [2400] [2600] [2667] [2800] [2933] [3000] [3200] [3467] [3600] [3733] [4000] [4200] [4267] [4400][4600] [4800] [5000]	Maximum Memory Frequency in Mhz. Must divide by 133 or 100 according to the refclk. In Gear2 must divide by 266 or 200. Lowest Gear2 speed is 2133

	[5200] [5400] [5600] [5800] [6000] [6200] [6400] [10000]	
HOB Buffer Size	<b>[Auto]</b> [1B] [1KB] [Max (assuming 63KB total HOB size)]	Size to set HOB Buffer
ECC Support	[Disabled] <b>[Enabled]</b>	Enable/disable DDR Ecc Support (Show as <u>SETUP_VOLATILE_DATA.PlatformFlavor</u> is not FlavorDesktop AND <u>SETUP_VOLATILE_DATA.PlatformFlavor</u> is not FlavorEmbedded AND <u>SETUP_VOLATILE_DATA.PlatformFlavor</u> is not FlavorUpServer AND <u>SETUP_VOLATILE_DATA.PlatformFlavor</u> is not FlavorWorkstation)
Max TOLUD	<b>[Dynamic]</b> [1 GB] [1.25 GB] [1.5 GB] [1.75 GB] [2 GB] [2.25 GB] [2.5 GB] [2.75 GB] [3 GB] [3.25 GB] [3.5 GB]	Maximum Value of TOLUD. Dynamic assignment would adjust TOLUD automatically based on largest MMIO length of installed graphic controller
SA GV	CPU_CFL is defined: <b>[Disabled]</b> [Fixed Low] [Fixed High] [Enabled]  else: [Disabled] [Fixed Low] [Fixed Mid] [Fixed High] <b>[Enabled]</b>	System Agent Geyserville. Fixed Low/Mid/High: SA GV disabled, MRC only runs tasks from Low, Mid, or High point.
First Point Frequency	<b>minimum = 0</b> <b>maximum = 0xFFFF</b> <b>step = 1</b> <b>default = 0</b>	Specify the frequency for the given point. 0 - MRC auto, Else a specific frequency as an integer: 1333
First Point Gear	<b>minimum = 0</b> <b>maximum = 4</b> <b>step = 1</b> <b>default = 0</b>	Gear ratio for this SAGV point. 0-Auto, 1-G1, 2-G2, 4-G4
Second Point Frequency	<b>minimum = 0</b> <b>maximum = 0xFFFF</b> <b>step = 1</b> <b>default = 0</b>	Specify the frequency for the given point. 0 - MRC auto, Else a specific frequency as an integer: 1333
Second Point Gear	<b>minimum = 0</b> <b>maximum = 4</b> <b>step = 1</b> <b>default = 0</b>	Gear ratio for this SAGV point. 0-Auto, 1-G1, 2-G2, 4-G4
Third Point Frequency	<b>minimum = 0</b> <b>maximum = 0xFFFF</b> <b>step = 1</b> <b>default = 0</b>	Specify the frequency for the given point. 0 - MRC auto, Else a specific frequency as an integer: 1333

Third Point Gear	<b>minimum = 0</b> <b>maximum = 4</b> <b>step = 1</b> <b>default = 0</b>	Gear ratio for this SAGV point. 0-Auto, 1-G1, 2-G2, 4-G4
Fourth Point Frequency	<b>minimum = 0</b> <b>maximum = 0xFFFF</b> <b>step = 1</b> <b>default = 0</b>	Specify the frequency for the given point. 0 - MRC auto, Else a specific frequency as an integer: 1333
Fourth Point Gear	<b>minimum = 0</b> <b>maximum = 4</b> <b>step = 1</b> <b>default = 0</b>	Gear ratio for this SAGV point. 0-Auto, 1-G1, 2-G2, 4-G4
Retrain on Fast Fail	[Disabled] <b>[Enabled]</b>	Restart MRC in Cold mode if SW MemTest fails during Fast flow.
DDR4_1DPC	[Disabled] [Enabled on DIMM0 only] [Enabled on DIMM1 only] <b>[Enabled]</b>	DDR4 1DPC performance feature for 2R DIMMs. Can be enabled on DIMM0 or DIMM1 only, or on both
Row Hammer Mode	<b>[Disabled]</b> [RFM] [pTRR]	Row Hammer Prevention Mode. RFM will fall back to pTRR if not available (Below option will show at this option not Disable)
RH LFSR0 Mask	[1/2^1] [1/2^2] [1/2^3] [1/2^4] [1/2^5] [1/2^6] [1/2^7] [1/2^8] [1/2^9] [1/2^10] <b>[1/2^11]</b> [1/2^12] [1/2^13] [1/2^14] [1/2^15]	LFSR0 mask for RH pTRR
RH LFSR1 Mask	[1/2^1] [1/2^2] [1/2^3] [1/2^4] [1/2^5] [1/2^6] [1/2^7] [1/2^8] [1/2^9] [1/2^10] <b>[1/2^11]</b> [1/2^12] [1/2^13] [1/2^14] [1/2^15]	LFSR1 mask for RH pTRR
MC Refresh Rate	<b>[NORMAL Refresh]</b> [1x Refresh][2x Refresh] [4x Refresh]	Select refresh rate on the MC
LPDDR ODT RttWr	<b>minimum = 0</b> <b>maximum = 0xFF</b> <b>step = 1</b> <b>default = 0</b>	Initial RttWr ODT override for LP4/5 in Ohms. Range 0x01 - 0xFF, default 0 = AUTO
LPDDR ODT RttCa	<b>minimum = 0</b> <b>maximum = 0xFF</b> <b>step = 1</b> <b>default = 0</b>	Initial RttCa ODT override for LP4/5 in Ohms. Range 0x01 - 0xFF, default 0 = AUTO
Refresh Watermarks	<b>[High]</b> [Low]	Sets Refresh Panic Watermark and Refresh High-Priority Watermark to HIGH or LOW values
Exit On Failure (MRC)	[Disabled] <b>[Enabled]</b>	Exit On Failure for MRC training steps

New Features 1 - MRC	<b>[Disabled]</b> [Enabled]	Enabling/Disabling Generic New Features 1
New Features 2 - MRC	<b>[Disabled]</b> [Enabled]	Enabling/Disabling Generic New Features 2
Ch Hash Override	<b>[Disabled]</b> [Enabled]	Override Channel Hash settings
Ch Hash Support	[Disabled] <b>[Enabled]</b>	Enable/Disable Channel Hash Support. 0 is Default(Auto) value - programs 2 in HASH_LSB_MASK, HASK_MASK value of 0x2094 for LPDDR4 and 0x30CC for NON-LPDDR4. NOTE: ONLY if Memory interleaved Mode
Ch Hash Mask	<b>minimum = 0x0000</b> <b>maximum = 0x3FFF</b> <b>step = 1</b> <b>default = 2096</b>	Set the BIT(s) to be included in the XOR function. NOTE BIT mask corresponds to BITS [19:6}
Ch Hash Interleaved Bit	[BIT6] [BIT7] <b>[BIT8]</b> [BIT9] [BIT10] [BIT11] [BIT12] [BIT13]	Select the BIT to be used for Channel Interleaved mode. NOTE: BIT7 will interlave the channels at a 2 cacheline granularity, BIT8 at 4 and BIT9 at 8
Extended Bank Hashing	Disabled] <b>[Enabled]</b>	Enable/disable Extended Bank Hashing.
Per Bank Refresh	[Disabled] <b>[Enabled]</b>	Enables and Disables the per bank refresh. This only impacts memory technologies that support PBR: LPDDR3, LPDDR4.
VC1 Read Metering	[Disabled] <b>[Enabled]</b>	Enable/Disable VC1 Read Metering Feature (RdMeter)
Strong Weak Leaker	<b>minimum = 1</b> <b>maximum = 7</b> <b>step = 1</b> <b>default = 7</b>	Value for StrongWkLeaker
Power Down Mode	<b>[Auto]</b> [No Power Down] [APD] [PPD-DLLoff]	CKE Power Down Mode Control
Pwr Down Idle Timer	<b>minimum = 0</b> <b>maximum = 255</b> <b>step = 1</b> <b>default = 0</b>	The minimum value should = to the worst case Roundtrip delay + Burst_Length. 0 means AUTO: 64 for ULX/ULT, 128 for DT/Halo
Page Close Idle Timeout	[Disabled] <b>[Enabled]</b>	Page Close Idle Timeout Control
Memory Scrambler	[Disabled] <b>[Enabled]</b>	Enable/Disable Memory Scrambler support.
Force ColdReset	[Enabled] <b>[Disabled]</b>	Force ColdReset OR Choose MrcColdBoot mode, when Coldboot is required during MRC execution. Note:

		If ME 5.0MB is present, ForceColdReset is required!
Controller 0, Channel 0 Control	[Disabled] <b>[Enabled]</b>	Controller 0, Channel 0 Control - Enable or Disable Controller 0, Channel 0.
Controller 0, Channel 1 Control	[Disabled] <b>[Enabled]</b>	Controller 0, Channel 1 Control - Enable or Disable Controller 0, Channel 1.
Controller 0, Channel 2 Control	[Disabled] <b>[Enabled]</b>	Controller 0, Channel 2 Control - Enable or Disable Controller 0, Channel 2.
Controller 0, Channel 3 Control	[Disabled] <b>[Enabled]</b>	Controller 0, Channel 3 Control - Enable or Disable Controller 0, Channel 3.
Controller 1, Channel 0 Control	[Disabled] <b>[Enabled]</b>	Controller 1, Channel 0 Control - Enable or Disable Controller 1, Channel 0.
Controller 1, Channel 1 Control	[Disabled] <b>[Enabled]</b>	Controller 1, Channel 1 Control - Enable or Disable Controller 1, Channel 1.
Controller 1, Channel 2 Control	[Disabled] <b>[Enabled]</b>	Controller 1, Channel 2 Control - Enable or Disable Controller 1, Channel 2.
Controller 1, Channel 3 Control	[Disabled] <b>[Enabled]</b>	Controller 1, Channel 3 Control - Enable or Disable Controller 1, Channel 3.
Force Single Rank	<b>[Disabled]</b> [Enabled]	When enabled, only Rank 0 will be used in each DIMM
In-Band ECC Support	<b>[Disabled]</b> [Enabled]	Enable/Disable In-Band ECC. Will be enabled if memory has symmetric configuration
Memory Remap	<b>[Enabled]</b> [Disabled]	Enable/Disable Memory Remap above 4GB
Time Measure	<b>[Disabled]</b> [Enabled]	Enable/Disable printing of the time it takes to execute MRC.
Fast Boot	[Disabled] <b>[Enabled]</b>	Enable/Disable fast path thru the MRC
Rank Margin Tool Per Task	<b>[Disabled]</b> [Enabled]	Enables/Disables RMT running at every major training step
Training Tracing	<b>[Disabled]</b> [Enabled]	Enables/Disables printing of the current trained state at every major training step.
Lpddr Mem WL Set	[Set A] <b>[Set B]</b>	Only applicable to LPDDR, Memory Write Latency Set selection (A is default, B will be used if memory devices support it)

BDAT ACPI Table Support	<b>[Disabled]</b> [Enabled]	Enables support for the BDAT ACPI table.
BDAT Memory Test Type	<b>[Rank Margin Tool Rank]</b> [Rank Margin Tool Bit] [Margin 2D]	Indicates the type of Memory Training data to populate into the BDAT ACPI table.
Rank Margin Tool Loop Count	<b>minimum = 0</b> <b>maximum = 32</b> <b>step = 1</b> <b>default = 0</b>	Specifies the Loop Count to be used during Rank Margin Tool Testing. 0 - AUTO
ECC DFT	<b>[Disabled]</b> [Enabled]	Enable/Disable ECC DFT feature
Write0	[Disabled] <b>[Enabled]</b>	Write0 feature for LP5/DDR5
Periodic DCC	<b>[Disabled]</b> [Enabled]	Enable / Disable Periodic DCC
LPMODE	<b>[Auto]</b> [Enabled] [Disabled]	Control LPMODE feature
PPR Enable	<b>[Disabled]</b> [Enabled]	PPR permanently repairs failed rows (if possible).

### 2.2.14.1 Memory Thermal Configuration

**Table 2-2-14-1. Memory Thermal Configuration**

BIOS Setting	Options	Description
Memory Thermal Configuration		
Memory Power and Thermal Throttling	(See Section 2.2.14.1.1)	
Memory Thermal Management	<b>[Disabled]</b> <b>[Enabled]</b>	Enable/Disable Memory Thermal Management. (Below options will show at this <u>option set Enabled</u> )
PECI Injected Temperature	<b>[Disabled]</b> [Enabled]	Enable/Disable memory temperatures to be injected to the processor via Peci.
EXTTS# via TS-on-Board	<b>[Disabled]</b> [Enabled]	Enable/Disable routing TS-on-Board's ALERT# and THERM# to EXTTS# pins on the PCH.
EXTTS# via TS-on-DIMM	<b>[Disabled]</b> [Enabled]	Enable/Disable routing TS-on-DIMM's ALERT# to EXTTS# pin on the PCH.
Virtual Temperature Sensor (VTS)	<b>[Disabled]</b> [Enabled]	Enable/Disable Virtual Temperature Sensor (VTS).

### 2.2.14.1.1 Memory Power and Thermal Throttling

**Table 2-2-14-1-1. Memory Power and Thermal Throttling**

BIOS Setting	Options	Description
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Memory Power and Thermal Throttling		
DDR PowerDown and idle counter	[PCODE] <b>[BIOS]</b>	BIOS: BIOS is in control of DDR CKE mode and idle timer value. PCODE: pcode will manage the modes.
For LPDDR Only: DDR PowerDown and idle counter	[PCODE] <b>[BIOS]</b>	For LPDDR Only: BIOS: BIOS is in control of DDR CKE mode and idle timer value. PCODE: pcode will manage the modes.
REFRESH_2X_MODE	<b>[Disabled]</b> [1- Enabled for WARM or HOT] [2- Enabled HOT only]	0- Disabled 1-iMC enables 2xRef when Warm and Hot 2- iMC enables 2xRef when Hot
SelfRefresh Enable	[Disabled] <b>[Enabled]</b>	Enable, Disable(Enable= Def)
SelfRefresh IdleTimer	<b>minimum = 512</b> <b>maximum = 65535</b> <b>step = 1</b> <b>default = 512</b>	range [64K-1;512]in DLCK800s, (512= Def)
Throttler CKEMin Defeature	<b>[Enabled]</b> [Disabled]	On, Off
Throttler CKEMin Timer	<b>minimum = 0</b> <b>maximum = 0xFF</b> <b>step = 1</b> <b>default = 0</b>	Timer value for CKEMin, range[255;0]. Req'd min of SC_ROUND_T + BYTE_LENGTH (4)
Allow Opp Ref Below Write Threshold	<b>[Disabled]</b> [Enabled]	Allow opportunistic refreshes while we don't exit power down.
Write Threshold	<b>minimum = 0</b> <b>maximum = 0x3F</b> <b>step = 1</b> <b>default = 0</b>	Number of writes that can be accumulated while CKE is low before CKE is asserted.
For LPDDR Only: Throttler CKEMin Defeature	<b>[Enabled]</b> [Disabled]	For LPDDR Only: On, Off (Show as <u>SETUP_VOLATILE_DATA.PlatformType</u> is TypeUitUlx)
For LPDDR Only: Throttler CKEMin Timer	<b>minimum = 0x0</b> <b>maximum = 0xFF</b> <b>step = 1</b> <b>default = 0</b>	For LPDDR Only: Timer value for CKEMin, range[255;0]. Req'd min of SC_ROUND_T + BYTE_LENGTH (4) (Show as <u>SETUP_VOLATILE_DATA.PlatformType</u> is TypeUitUlx)

### 2.2.14.2 Memory Training Algorithms

**Table 2-2-14-2. Memory Training Algorithms**

BIOS Setting	Options	Description
Early Command Training	[Disabled] <b>[Enabled]</b>	Early Command Training
SenseAmp Offset Training	<b>[Disabled]</b> [Enabled]	SenseAmp Offset Training

Early ReadMPR Timing Centering 2D	[Disabled] <b>[Enabled]</b>	None
Read MPR Training	<b>[Disabled]</b> [Enabled]	Read MPR Training
Receive Enable Training	[Disabled] <b>[Enabled]</b>	Receive Enable Training
Jedec Write Leveling	[Disabled] <b>[Enabled]</b>	Jedec Write Leveling
Early Write Time Centering 2D	[Disabled] <b>[Enabled]</b>	Early Write Time Centering 2D
Early Read Time Centering 2D	CPU_CFL is defined: [Disabled] <b>[Enabled]</b>  else: [Enabled] <b>[Disabled]</b>	None
Write Timing Centering 1D	[Disabled] <b>[Enabled]</b>	Write Timing Centering 1D
Write Voltage Centering 1D	[Disabled] <b>[Enabled]</b>	None
Read Timing Centering 1D	[Disabled] <b>[Enabled]</b>	Read Timing Centering 1D
Dimm ODT Training*	[Disabled] <b>[Enabled]</b>	Dimm On-Die Termination Training (Below options can be set at this option set Enabled)
Max RTT_WR	<b>[ODT Off]</b> [120 Ohms]	Caps the maximum RTT_WR in power training.
DIMM RON Training*	<b>[Disabled]</b> [Enabled]	DIMM RON Training
Write Drive Strength/Equalization 2D*	[Disabled] <b>[Enabled]</b>	
Write Slew Rate Training*	[Disabled] <b>[Enabled]</b>	Write Slew Rate Training
Read ODT Training*	[Disabled] <b>[Enabled]</b>	Read On-Die Termination Training
Read Equalization Training*	CPU_CFL is defined: [Disabled] <b>[Enabled]</b>  else: <b>[Disabled]</b> [Enabled]	Read Equalization Training
Read Amplifier Training*	[Disabled] <b>[Enabled]</b>	Read Amplifier Training
Write Timing Centering 2D	[Disabled] <b>[Enabled]</b>	Write Dq-Dqs Timing Centering 2D
Read Timing Centering 2D	[Disabled] <b>[Enabled]</b>	Read Dq-Dqs Timing Centering 2D
Command Voltage Centering	[Disabled] <b>[Enabled]</b>	Command Voltage Centering

Write Voltage Centering 2D	[Disabled] <b>[Enabled]</b>	Write Voltage Centering 2D
Read Voltage Centering 2D	[Disabled] <b>[Enabled]</b>	Read Voltage Centering 2D
Late Command Training	[Disabled] <b>[Enabled]</b>	Late Command Training
Round Trip Latency	[Disabled] <b>[Enabled]</b>	Round Trip Latency Training
Turn Around Timing Training	<b>[Disabled]</b> [Enabled]	Turn Around Timing Training
CMD CTL CLK Slew Rate	[Disabled] <b>[Enabled]</b>	CMD CTL CLK Slew Rate
CMD/CTL DS & E 2D	[Disabled] <b>[Enabled]</b>	CMD/CTL DS & E 2D
Read Voltage Centering 1D	[Disabled] <b>[Enabled]</b>	Read Voltage Centering 1D
TxDqTCO Comp Training*	[Disabled] <b>[Enabled]</b>	TxDqTCO Comp Training*
ClkTCO Comp Training*	[Disabled] <b>[Enabled]</b>	ClkTCO Comp Training*
TxDqsTCO Comp Training*	[Disabled] <b>[Enabled]</b>	TxDqsTCO Comp Training*
VccDLL Bypass Training	[Disabled] <b>[Enabled]</b>	VccDLL Bypass Training
CMD/CTL Drive Strength Up/Dn 2D	[Disabled] <b>[Enabled]</b>	CMD/CTL Drive Strength Up/Dn 2D
DIMM CA ODT Training	[Disabled] <b>[Enabled]</b>	DIMM CA ODT Training
PanicVttDnLp Training*	[Disabled] <b>[Enabled]</b>	PanicVttDnLp Training*
Read Vref Decap Training*	[Disabled] <b>[Enabled]</b>	Read Vref Decap Training*
Vddq Training	<b>[Disabled]</b> [Enabled]	Vddq Training
Duty Cycle Correction Training	[Disabled] <b>[Enabled]</b>	Duty Cycle Correction Training
Rank Margin Tool Per Bit	<b>[Disabled]</b> [Enabled]	Rank Margin Tool Per Bit
DIMM DFE Training	[Disabled] <b>[Enabled]</b>	DIMM DFE Training
Tx Dqs Dcc Training	[Disabled] <b>[Enabled]</b>	Tx Dqs Dcc Training
Rank Margin Tool	<b>[Disabled]</b> [Enabled]	Rank Margin Tool Training
Memory Test	<b>[Disabled]</b> [Enabled]	Memory Test Training

DIMM SPD Alias Test	<b>[Disabled]</b> [Enabled]	Test to determine if the SPD has been corrupted to cause memory aliasing.
Receive Enable Centering 1D		Receive Enable Centering 1D
Retrain Margin Check	<b>[Disabled]</b> [Enabled]	Retrain Margin Check
Write Drive Strength Up/Dn independently	[Disabled] <b>[Enabled]</b>	Write Drive Strength Up/Dn independently
Margin Check Limit	<b>[Disabled]</b> [L1] [L2] [Both]	Checks Margin to Limit to see if next boot memory needs to be retrain
Margin Limit Check L2	<b>default = 100</b>	L2 check threshold is scale of L1 check. Ex. 200 is 2 x L1 Check

## 2.2.15 System Agent (SA) Configuration

**Table 2-2-15. System Agent (SA) Configuration**

BIOS Setting	Options	Description
System Agent (SA) Configuration		
VT-d	No options	VT-d capability
Graphics Configuration	(See Section 2.2.15.1)	Graphics Configuration
DMI/OPI Configuration	(See Section 2.2.15.2)	Control various DMI functions.
TCSS setup menu	(See Section 2.2.15.3)	TCSS Configuration settings
VMD setup menu	(See Section 2.2.15.4)	VMD Configuration settings
Display setup menu	(See Section 2.2.15.5)	Display Configuration settings
PCI Express Configuration	(See Section 2.2.15.6)	PCI Express Configuration settings
Stop Grant Configuration	<b>[Auto]</b> [manual]	Automatic/Manual stop grant configuration
Number of Stop Grant Cycles	<b>minimum = 1</b> <b>maximum = 0x3f</b> <b>step = 0</b> <b>default = 1</b>	Selects number of Stop-Grant cycles. (Show as <u>Stop Grant Configuration</u> set to manual)
VT-d	[Disabled] <b>[Enabled]</b>	VT-d capability
Control Iommu Pre-boot Behavior	[Disable IOMMU] <b>[Enable IOMMU during boot]</b>	Enable IOMMU in Pre-boot environment (If DMAR table is installed in DXE and If VTD_INFO_PPI is installed in PEI.)
X2APIC Opt Out	[Enabled] <b>[Disabled]</b>	Enable/Disable X2APIC_OPT_OUT bit

		(Show as <u>SETUP_VOLATILE_DATA.VTdAvailable</u> is not 0 OR <u>SA_SETUP.EnableVtd</u> is not 0 <u>SETUP_CPU_FEATURES.LocalX2ApicAvailable</u> is not 0)
DMA Control Guarantee	<b>[Enable]</b> [Disable]	Enable/Disable Dma Control Guarantee bit
IGD VTD Enable	<b>[Enable]</b> [Disable]	Enable/Disable IGD VTD.
IOP VTD Enable	<b>[Enable]</b> [Disable]	Enable/Disable IOP VTD.
Control Iommu Pre-boot Behavior	[Disable IOMMU] <b>[Enable IOMMU during boot without exception list]</b>	Enable dTBT and PCH USB topology IOMMU in Pre-boot environment (If DMAR table is installed in DXE and If VTD_INFO_PPI is installed in PEI.) TBT tree won't be included in the exception list.
CHAP Device (B0:D7:F0)	<b>[Disabled]</b> [Enabled]	Enable/Disable SA CHAP Device.
Thermal Device (B0:D4:F0)	<b>[Disabled]</b> [Enabled]	Enable/Disable SA Thermal Device.
Cpu CrashLog (Device 10)	[Disabled] <b>[Enabled]</b>	Enable/Disable Cpu CrashLog Device.
GNA Device (B0:D8:F0)	[Disabled] <b>[Enabled]</b>	Enable/Disable SA GNA Device.
CRID Support	<b>[Disabled]</b> [Enabled]	Enable/Disable CRID control for Intel SIPP
WRC Feature	<b>[Disabled]</b> [Enabled]	Enable/Disable SA WRC(Write Cache) Feature of IOP. When enabled, supports IO devices allocating onto the ring and into LLC.
Above 4GB MMIO BIOS assignment	[Disabled] <b>[Enabled]</b>	Enable/Disable above 4GB MemoryMappedIO BIOS assignment This is enabled automatically when Aperture Size is set to 2048MB. (Show as <u>SA_SETUP.ApertureSize</u> is not 15 <u>SystemConfig.BootType</u> is not 0 1)
MIPI Camera Configuration	(See Section 2.2.15.7)	MIPI Camera Configuration
eDRAM Mode	[SW Mode eDRAM Off] [ SW Mode eDRAM On] <b>[eDRAM HW Mode]</b>	SW Mode eDRAM On or eDRAM Off (Show as <u>CPU_SETUP_VOLATILE_DATA.EdramSupported</u> is not 1);

### 2.2.15.1 Graphics Configuration

**Table 2-2-15-1. Graphics Configuration**

BIOS Setting	Options	Description
Graphics Configuration		

Graphics Turbo IMON Current	<b>minimum = 14</b> <b>maximum = 31</b> <b>step = 1</b> <b>default = 31</b>	Graphics turbo IMON current values supported (14-31) (Show as <u>SETUP_VOLATILE_DATA.PlatformFlavor</u> is not FlavorUpServer)
Skip Scanning of External Gfx Card	<b>[Disabled]</b> [Enabled]	If Enable, it will not scan for External Gfx Card on PEG and PCH PCIE Ports
Primary Display	SG support: <b>[Auto]</b> [IGFX] [PCI] [SG] else: <b>[Auto]</b> [IGFX] [PCI] [SG]	Select which of IGFX/PEG/PCI Graphics device should be Primary Display Or select HG for Hybrid Gfx.
Select PCIE Card	<b>[Auto]</b> [Elk Creek 4] [PEG Eval]	Select the card used on the platform Auto: Skip GPIO based Power Enable to dGPU Elk Creek 4: DGPU Power Enable = ActiveLow PEG Eval: DGPU Power Enable = ActiveHigh
Internal Graphics	<b>[Auto]</b> [Disabled] [Enabled]	Keep IGFX enabled based on the setup options.
GTT Size	[2MB] [4MB] <b>[8MB]</b>	Select the GTT Size
Aperture Size	[128MB] <b>[256MB]</b> [512MB] [1024MB] [2048MB]	Select the Aperture Size Note : Above 4GB MMIO BIOS assignment is automatically enabled when selecting 2048MB aperture. To use this feature, please disable CSM Support.
PSMI SUPPORT	<b>[Disabled]</b> [Enabled]	PSMI Enable/Disable (Below options will show at this option set Enabled)
PSMI Region Size	<b>[32MB]</b> [288MB] [544MB] [800MB] [1024MB]	Select the PSMI Region Size : Range from 32MB to 1024MB
DVMT Pre-Allocated	[0M] [32M] [64M] [4M] [8M] [12M] [16M] [20M] [24M] [28M] [32M/F7] [36M] [40M][44M][48M][52M][56M] <b>[60M]</b>	Select DVMT 5.0 Pre-Allocated (Fixed) Graphics Memory size used by the Internal Graphics Device.
DVMT Total Gfx Mem	[128M] <b>[256M]</b> [MAX]	Select DVMT5.0 Total Graphic Memory size used by the Internal Graphics Device.
Intel Graphics Pei Display Peim	<b>[Disabled]</b> [Enabled]	Enable/Disable Pei (Early) Display
ALS Support	[Enabled] <b>[Disabled]</b>	Valid only for ACPI. Legacy = ALS Support through the IGFX INT10 function. ACPI = ALS support through an ACPI ALS driver.

VDD Enable	[Disabled] <b>[Enabled]</b>	Enable/Disable forcing of VDD in the BIOS (Show as <u>SETUP_VOLATILE_DATA.PlatformFlavor</u> is not FlavorUpServer)
Configure GT for use	<b>[Enabled]</b> [Disabled]	Enable/Disable GT configuration in BIOS
RC1p Support	[Enabled] <b>[Disabled]</b>	Enable/Disable RC1p support. If RC1p is enabled, send a RC1p frequency request to PMA based other conditions being met
PAVP Enable	<b>[Enabled]</b> [Disabled]	Enable/Disable PAVP
Cdynmax Clamping Enable	CPU_CFL is defined: <b>[Enabled]</b> [Disabled] else: [Enabled] <b>[Disabled]</b>	Enable/Disable Cdynmax Clamping
Cd Clock Frequency	CPU_CFL is defined: [307.2 Mhz] [556.8 Mhz] [652.8 Mhz] <b>[Max CdClock freq based on Reference Clk]</b>	Select the highest Cd Clock frequency supported by the platform
VBT Select	<b>[Disabled]</b> [Enabled]	Select VBT for GOP Driver\nSelect Vbt to MIPI if any of the Display has MIPI
Enable Display Audio Link in Pre-OS	<b>[Disabled]</b> [Enabled]	Enable : Display Audio Link will be enabled in Pre-OS.\nDisabled : Display Audio Link will be disabled in Pre-OS.
IUER Button Enable	<b>[Disabled]</b> [Enabled]	Enable/Disable IUER Button Functionality
LCD Control	(See Section 2.2.15.1.1)	LCD Control.(Show as PlatformFlavor notFlavorUpServerand BootType is not 2)
Intel(R) Ultrabook Event Support	(See Section 2.2.15.1.2)	Intel(R) Ultrabook Event Support (Show as PlatformFlavor is FlavorMobile)

### 2.2.15.1.1 LCD Control

**Table 2-2-14-1-1. LCD Control**

BIOS Setting	Options	Description
LCD Control		
Primary IGFX Boot Display	<b>[VBIOS Default]</b> [EFP] [LFP] [EFP3] [EFP2] [EFP4]	Select the Video Device which will be activated during POST. This has no effect if external graphics present. Secondary boot display selection will appear based on your selection. VGA modes will be supported only on primary display.

Secondary IGFX Boot Display	<b>[Disable]</b> [EFP] [EFP3] [EFP2] [EFP4]	Select Secondary Display Device. (Show as Primary IGFX Boot Display is not VBIOS Default)
LCD Panel Type	<b>[VBIOS Default]</b> [640x480 LVDS] [800x600 LVDS] [1024x768 LVDS] [1280x1024 LVDS] [1400x1050 LVDS1] [1400x1050 LVDS2] [1600x1200 LVDS] [1280x768 LVDS] [1680x1050 LVDS] [1920x1200 LVDS] [1600x900 LVDS] [1280x800 LVDS] [1280x600 LVDS] [1280x600 LVDS] [2048x1536 LVDS] [1366x768 LVDS]	Select LCD panel used by Internal Graphics Device by selecting the appropriate setup item.
Panel Scaling	<b>[Auto]</b> [Off] [Force Scaling]	Select the LCD panel scaling option used by the Internal Graphics Device.
Backlight Control	[PWM Inverted] <b>[PWM Normal]</b>	Back Light Control Setting
Active LFP	[No eDP] <b>[eDP Port-A]</b>	Select the Active LFP Configuration. No LVDS:VBIOS does not enable LVDS. Int-LVDS:VBIOS enables LVDS driver by Integrated encoder. SDVO LVDS:VBIOS enables LVDS driver by SDVO encoder. eDP Port-A:LFP Driven by Int-DisplayPort encoder from Port-A. eDP Port-D:LFP Driven by Int-DisplayPort encoder from Port-D(through PCH).
Panel Color Depth	<b>[18 Bit]</b> [24Bit]	Select the LFP Panel Color Depth
Backlight Brightness	<b>minimum = 0</b> <b>maximum = 255</b> <b>step = 0</b> <b>default = 255</b>	Set VBIOS Brightness. Range : 0-255.

### 2.2.14.1.2 Intel(R) Ultrabook Event Support

**Table 2-2-14-1-2. Intel(R) Ultrabook Event Support**

BIOS Setting	Options	Description
Intel(R) Ultrabook Event Support		

IUER Slate Enable	<b>[Disabled]</b> [Enabled]	Enable/Disable IUER Slate Functionality (Below options will show at this option set Enabled)
Slate Mode boot value	[Slate Mode] <b>[Laptop Mode]</b>	Choose Slate or Laptop as boot mode.
Slate Mode on S3 and S4 resume	<b>[No change]</b> [Toggle]	Keep it the same as Sx entry or toggle it.
IUER Dock Enable	<b>[Disabled]</b> [Enabled]	Enable/Disable IUER Dock Functionality (Below options will show at this option set Enabled)
Dock Mode boot value	<b>[Undocked]</b> [Docked]	Choose Docked or Undocked as boot mode.
Dock Mode upon S3 and S4 resume	<b>[No change]</b> [Toggle]	Keep it the same as Sx entry or toggle it.

### 2.2.14.2 DMI/OPI Configuration

**Table 2-2-14-2. DMI/OPI Configuration**

BIOS Setting	Options	Description
DMI/OPI Configuration		
(Show as <i>SETUP VOLATILE DATA.PlatformType</i> is not TypeTrad)		
DMI Max Link Speed	<b>[Auto]</b> [Gen1][Gen2][Gen3]	Set DMI Speed Gen1/Gen2/Gen3.
CDR Relock for CPU DMI	[Disabled] <b>[Enabled]</b>	Enable/Disable CDR Relock"
DMI Gen3 Eq Phase 2	[Disabled] [Enabled] <b>[Auto]</b>	Perform Gen3 Equalization Phase 2.
DMI Gen3 Eq Phase 3 Method	<b>[Auto]</b> [Adaptive Hardware Equalization] [Adaptive Software Equalization] [Static Equalization] [Disabled]	Select Method for Gen3 Equalization Phase 3.
DMI Gen3 ASPM	[Disabled] [Auto] [ASPM L0s] <b>[ASPM L1]</b> [ASPM L0sL1]	DMI Gen3 ASPM Support
DMI ASPM	[Disabled] [Auto] [ASPM L0s] <b>[ASPM L1]</b> [ASPM L0sL1]	DMI ASPM Support
DMI Gen3 L1 Exit Latency	<b>minimum = 0</b> <b>maximum = 7</b> <b>step = 1</b> <b>default = 4</b>	DMI Gen3 L1 Exit Latency
New FOM for CPU DMI	[Enabled] <b>[Disabled]</b>	None

Program Static Phase1 Eq	[Disabled] <b>[Enabled]</b>	Program Phase1 Presets/CTLEp.
Gen3 Root Port Preset value for each Lane	(See Section 2.2.15.2.1)	Root Port preset value per lane for Gen3 Equalization. (Show as ProgramStaticPhase1Eq is Enable)
Gen3 Endpoint Preset value for each Lane	(See Section 2.2.15.2.2)	Endpoint preset value per lane for Gen3 Equalization. (Show as ProgramStaticPhase1Eq is Enable)
Gen3 Endpoint Hint value for each Lane	(See Section 2.2.15.2.3)	Endpoint Hint value per lane for Gen3 Equalization. (Show as ProgramStaticPhase1Eq is Enable)
Gen3 RxCTLE Control	(See Section 2.2.15.2.4)	Gen3 RxCTLE Control per Bundle.
DMI Link ASPM Control	[Disabled] [L0s] <b>[L1]</b> [L0sL1]	Enable/Disable the control of Active State Power Management on SA side of the DMI Link.
DMI Extended Sync Control	[Enabled] <b>[Disabled]</b>	Enable DMI Extended Synchronization.
DMI De-emphasis Control	[-6 dB] <b>[-3.5 dB]</b>	Configure the De-emphasis control on DMI
DMI IOT	[Enabled] <b>[Disabled]</b>	Enable/Disable DMI IOT

### 2.2.15.2.1 Gen3 Root Port Preset value for each Lane

**Table 2-2-15-2-1. Gen3 Root Port Preset value for each Lane**

BIOS Setting	Options	Description
Gen3 Root Port Preset value for each Lane		
Lane 0	<b>minimum = 0</b> <b>maximum = 9</b> <b>step = 1</b> <b>default = 4</b>	Value for Lane 0
Lane 1	<b>minimum = 0</b> <b>maximum = 9</b> <b>step = 1</b> <b>default = 4</b>	Value for Lane 1
Lane 2	<b>minimum = 0</b> <b>maximum = 9</b> <b>step = 1</b> <b>default = 4</b>	Value for Lane 2
Lane 3	<b>minimum = 0</b> <b>maximum = 9</b> <b>step = 1</b> <b>default = 4</b>	Value for Lane 3

Lane 4 (Except CFL)	<b>minimum = 0</b> <b>maximum = 9</b> <b>step = 1</b> <b>default = 4</b>	Value for Lane 4
Lane 5 (Except CFL)	<b>minimum = 0</b> <b>maximum = 9</b> <b>step = 1</b> <b>default = 4</b>	Value for Lane 5
Lane 6 (Except CFL)	<b>minimum = 0</b> <b>maximum = 9</b> <b>step = 1</b> <b>default = 4</b>	Value for Lane 6
Lane 7 (Except CFL)	<b>minimum = 0</b> <b>maximum = 9</b> <b>step = 1</b> <b>default = 4</b>	Value for Lane 7

### 2.2.15.2.2 Gen3 Endpoint Preset value for each Lane

**Table 2-2-15-2-2. Gen3 Endpoint Preset value for each Lane**

BIOS Setting	Options	Description
Gen3 Endpoint Preset value for each Lane		
Lane 0	<b>minimum = 0</b> <b>maximum = 9</b> <b>step = 1</b> <b>default = 7</b>	Value for Lane 0
Lane 1	<b>minimum = 0</b> <b>maximum = 9</b> <b>step = 1</b> <b>default = 7</b>	Value for Lane 1
Lane 2	<b>minimum = 0</b> <b>maximum = 9</b> <b>step = 1</b> <b>default = 7</b>	Value for Lane 2
Lane 3	<b>minimum = 0</b> <b>maximum = 9</b> <b>step = 1</b> <b>default = 7</b>	Value for Lane 3
Lane 4 (Except CFL)	<b>minimum = 0</b> <b>maximum = 9</b> <b>step = 1</b> <b>default = 7</b>	Value for Lane 4
Lane 5 (Except CFL)	<b>minimum = 0</b> <b>maximum = 9</b> <b>step = 1</b> <b>default = 7</b>	Value for Lane 5
Lane 6 (Except CFL)	<b>minimum = 0</b> <b>maximum = 9</b>	Value for Lane 6

	<b>step = 1</b> <b>default = 7</b>	
Lane 7 (Except CFL)	<b>minimum = 0</b> <b>maximum = 9</b> <b>step = 1</b> <b>default = 7</b>	Value for Lane 7

### 2.2.15.2.3 Gen3 Endpoint Hint value for each Lane

**Table 2-2-15-2-3. Gen3 Endpoint Hint value for each Lane**

BIOS Setting	Options	Description
Gen3 Endpoint Hint value for each Lane		
Lane 0	<b>minimum = 0</b> <b>maximum = 6</b> <b>step = 1</b> <b>default = 2</b>	Value for Lane 0
Lane 1	<b>minimum = 0</b> <b>maximum = 6</b> <b>step = 1</b> <b>default = 2</b>	Value for Lane 1
Lane 2	<b>minimum = 0</b> <b>maximum = 6</b> <b>step = 1</b> <b>default = 2</b>	Value for Lane 2
Lane 3	<b>minimum = 0</b> <b>maximum = 6</b> <b>step = 1</b> <b>default = 2</b>	Value for Lane 3
Lane 4 (Except CFL)	<b>minimum = 0</b> <b>maximum = 6</b> <b>step = 1</b> <b>default = 2</b>	Value for Lane 4
Lane 5 (Except CFL)	<b>minimum = 0</b> <b>maximum = 6</b> <b>step = 1</b> <b>default = 2</b>	Value for Lane 5
Lane 6 (Except CFL)	<b>minimum = 0</b> <b>maximum = 6</b> <b>step = 1</b> <b>default = 2</b>	Value for Lane 6
Lane 7 (Except CFL)	<b>minimum = 0</b> <b>maximum = 6</b> <b>step = 1</b> <b>default = 2</b>	Value for Lane 7

### 2.2.15.2.4 Gen3 RxCTLE Control

**Table 2-2-15-2-4. Gen3 RxCTLE Control**

BIOS Setting	Options	Description
Gen3 RxCTLE Control		
Bundle0	<b>minimum = 0</b> <b>maximum = 15</b> <b>step = 1</b> <b>default = 3</b>	Gen3 RxCTLE setting for Bundle0 (Lane0, Lane1)
Bundle1	<b>minimum = 0</b> <b>maximum = 15</b> <b>step = 1</b> <b>default = 3</b>	Gen3 RxCTLE setting for Bundle1 (Lane2, Lane3)
Bundle2 (Except CFL)	<b>minimum = 0</b> <b>maximum = 15</b> <b>step = 1</b> <b>default = 0</b>	Gen3 RxCTLE setting for Bundle2 (Lane4, Lane5)
Bundle3 (Except CFL)	<b>Minimum = 0</b> <b>maximum = 15</b> <b>step = 1</b> <b>default = 0</b>	Gen3 RxCTLE setting for Bundle3 (Lane6, Lane7)

### 2.2.15.3 PEG Port Configuration

**Table 2-2-15-3. PEG Port Configuration**

BIOS Setting	Options	Description
PEG Port Configuration		
PEG 0:1:0	Not Present	PEG 0:1:0 Link and Speed Information
Enable Root Port	[Disabled] [Enabled] <b>[Auto]</b>	Enable or Disable the Root Port
Max Link Speed	<b>[Auto]</b> [Gen1] [Gen2] [Gen3]	Configure PEG 0:1:0 Max Speed
Max Link Width	<b>[Auto]</b> [Force X1] [Force X2] [Force X4] [Force X8]	Force PEG link to retrain to X1/2/4/8
Power Down Unused Lanes	[Disabled] <b>[Auto]</b>	<u>Power Down Unused Lanes.</u> <u>Disabled: No power saving</u> <u>Auto: Bios will power down unused lanes based on the max possible link width</u>
Gen3 Eq Phase 2	[Disabled] [Enabled] <b>[Auto]</b>	Perform Gen3 Equalization Phase 2
Gen3 Eq Phase 3 Method	<b>[Auto]</b> [Adaptive Hardware Equalization] [Adaptive Software Equalization] [Static Equalization] [Disabled]	Select Method for Gen3 Equalization Phase 3

ASPM	[Disabled] <b>[Auto]</b> [L0s] [L1] [L0sL1]	Control ASPM support for the PEG 0. This has no effect if PEG is not the currently active device.
ASPM L0s	[Root Port Only] [Endpoint Port Only] <b>[Both Root and Endpoint Ports]</b>	PEG0: Enable PCIe ASPM L0s.
De-emphasis Control	[-6dB] <b>[-3.5dB]</b>	PEG0: Configure the De-emphasis control on PEG
OBFF	[Disabled] <b>[Enabled]</b>	CPU PEG2 (0,1,0) OBFF Enable/Disable
LTR	[Disabled] <b>[Enabled]</b>	CPU PEG2 (0,1,0) Latency Reporting Enable/Disable
PEG0 Slot Power Limit Value	<b>minimum = 0</b> <b>maximum = 255</b> <b>step = 1</b> <b>default = 75</b>	Sets the upper limit on power supplied by slot. Power limit (in Watts) is calculated by multiplying this value by the Slot Power Limit Scale. Values 0-255
PEG0 Slot Power Limit Scale	<b>[1.0x]</b> [0.1x] [0.01x] [0.001x]	Select the scale used for the Slot Power Limit Value.
PEG0 Physical Slot Number	<b>minimum = 0</b> <b>maximum = 8191</b> <b>step = 1</b> <b>default = 1</b>	Set the physical slot number attached to this Port. The number has to be globally unique within the chassis. Values 0-8191
PEG0 Hotplug	<b>[Disabled]</b> [Enabled]	PCI Express Hot Plug Enable/Disable
Extra Bus Reserved	<b>minimum = 0</b> <b>maximum = 7</b> <b>step = 1</b> <b>default = 0</b>	Extra Bus Reserved (0-7) for bridges behind this Root Bridge.
Reserved Memory	<b>minimum = 1</b> <b>maximum = 20</b> <b>step = 1</b> <b>default = 10</b>	Reserved Memory for this Root Bridge (1-4096) MB
Reserved I/O	<b>minimum = 4</b> <b>maximum = 20</b> <b>step = 4</b> <b>default = 4</b>	Reserved I/O (4K/8K/12K/16K/20K) Range for this Root Bridge.
PEG 0:1:1	Not Present	PEG 0:1:1 Link and Speed Information
Enable Root Port	[Disabled] [Enabled] <b>[Auto]</b>	Enable or Disable the Root Port
Max Link Speed	<b>[Auto]</b> [Gen1] [Gen2] [Gen3]	Configure PEG 0:1:1 Max Speed
Max Link Width	<b>[Auto]</b> [Force X1] [Force X2] [Force X4] [Force X8]	Force PEG link to retrain to X1/2/4/8
Power Down Unused Lanes	[Disabled] <b>[Auto]</b>	Power Down Unused Lanes. Disabled: No power saving

		Auto: Bios will power down unused lanes based on the max possible link width
Gen3 Eq Phase 2	[Disabled] [Enabled] <b>[Auto]</b>	Perform Gen3 Equalization Phase 2
Gen3 Eq Phase 3 Method	<b>[Auto]</b> [Adaptive Hardware Equalization] [Adaptive Software Equalization] [Static Equalization] [Disabled]	Select Method for Gen3 Equalization Phase 3
ASPM	[Disabled] <b>[Auto]</b> [L0s] [L1] [L0sL1]	Control ASPM support for the PEG 1. This has no effect if PEG is not the currently active device.
ASPM L0s	[Root Port Only] [Endpoint Port Only] <b>[Both Root and Endpoint Ports]</b>	PEG1: Enable PCIe ASPM L0s.
De-emphasis Control	[-6dB] <b>[-3.5dB]</b>	PEG1: Configure the De-emphasis control on PEG
OBFF	[Disabled] <b>[Enabled]</b>	CPU PEG1 (0,1,1) OBFF Enable/Disable
LTR	[Disabled] <b>[Enabled]</b>	CPU PEG1 (0,1,1) Latency Reporting Enable/Disable
PEG1 Slot Power Limit Value	<b>minimum = 0</b> <b>maximum = 255</b> <b>step = 1</b> <b>default = 75</b>	Sets the upper limit on power supplied by slot. Power limit (in Watts) is calculated by multiplying this value by the Slot Power Limit Scale. Values 0-255
PEG1 Slot Power Limit Scale	<b>[1.0x]</b> [0.1x] [0.01x] [0.001x]	Select the scale used for the Slot Power Limit Value.
PEG1 Physical Slot Number	<b>minimum = 0</b> <b>maximum = 8191</b> <b>step = 1</b> <b>default = 2</b>	Set the physical slot number attached to this Port. The number has to be globally unique within the chassis. Values 0-8191
PEG1 Hotplug	<b>[Disabled]</b> [Enabled]	PCI Express Hot Plug Enable/Disable
Extra Bus Reserved	<b>minimum = 0</b> <b>maximum = 7</b> <b>step = 1</b> <b>default = 0</b>	Extra Bus Reserved (0-7) for bridges behind this Root Bridge.
Reseved Memory	<b>minimum = 1</b> <b>maximum = 20</b> <b>step = 1</b> <b>default = 10</b>	Reserved Memory for this Root Bridge (1-4096) MB
Reserved I/O	<b>minimum = 4</b> <b>maximum = 20</b> <b>step = 4</b>	Reserved I/O (4K/8K/12K/16K/20K) Range for this Root Bridge.

	<b>default = 4</b>	
PEG 0:1:2	Not Present	PEG 0:1:2 Link and Speed Information
Enable Root Port	[Disabled] [Enabled] <b>[Auto]</b>	Enable or Disable the Root Port
Max Link Speed	<b>[Auto]</b> [Gen1] [Gen2] [Gen3]	Configure PEG 0:1:2 Max Speed
Max Link Width	<b>[Auto]</b> [Force X1] [Force X2] [Force X4] [Force X8]	Force PEG link to retrain to X1/2/4/8
Power Down Unused Lanes	[Disabled] <b>[Auto]</b>	Power Down Unused Lanes. Disabled: No power saving Auto: Bios will power down unused lanes based on the max possible link width
Gen3 Eq Phase 2	[Disabled] [Enabled] <b>[Auto]</b>	Perform Gen3 Equalization Phase 2
Gen3 Eq Phase 3 Method	<b>[Auto]</b> [Adaptive Hardware Equalization] [Adaptive Software Equalization] [Static Equalization] [Disabled]	Select Method for Gen3 Equalization Phase 3
ASPM	[Disabled] <b>[Auto]</b> [L0s] [L1] [L0sL1]	Control ASPM support for the PEG 2. This has no effect if PEG is not the currently active device.
ASPM L0s	[Root Port Only] [Endpoint Port Only] <b>[Both Root and Endpoint Ports]</b>	PEG2: Enable PCIe ASPM L0s.
De-emphasis Control	[-6dB] <b>[-3.5dB]</b>	PEG2: Configure the De-emphasis control on PEG
OBFF	[Disabled] <b>[Enabled]</b>	CPU PEG2 (0,1,2) OBFF Enable/Disable
LTR	[Disabled] <b>[Enabled]</b>	CPU PEG2 (0,1,2) Latency Reporting Enable/Disable
PEG2 Slot Power Limit Value	<b>minimum = 0</b> <b>maximum = 255</b> <b>step = 1</b> <b>default = 75</b>	Sets the upper limit on power supplied by slot. Power limit (in Watts) is calculated by multiplying this value by the Slot Power Limit Scale. Values 0-255
PEG2 Slot Power Limit Scale	<b>[1.0x]</b> [0.1x] [0.01x] [0.001x]	Select the scale used for the Slot Power Limit Value.
PEG2 Physical Slot Number	<b>minimum = 0</b> <b>maximum = 8191</b> <b>step = 1</b> <b>default = 3</b>	Set the physical slot number attached to this Port. The number has to be globally unique within the chassis. Values 0-8191

PEG2 Hotplug	<b>[Disabled]</b> [Enabled]	PCI Express Hot Plug Enable/Disable
Extra Bus Reserved	<b>minimum = 0</b> <b>maximum = 7</b> <b>step = 1</b> <b>default = 0</b>	Extra Bus Reserved (0-7) for bridges behind this Root Bridge.
Reseved Memory	<b>minimum = 1</b> <b>maximum = 20</b> <b>step = 1</b> <b>default = 10</b>	Reserved Memory for this Root Bridge (1-4096) MB
Reserved I/O	<b>minimum = 4</b> <b>maximum = 20</b> <b>step = 4</b> <b>default = 4</b>	Reserved I/O (4K/8K/12K/16K/20K) Range for this Root Bridge.
PEG 0:6:0	Not Present	PEG 0:6:0 Link and Speed Information
Enable Root Port	[Disabled] [Enabled] <b>[Auto]</b>	Enable or Disable the Root Port
Max Link Speed	<b>[Auto]</b> [Gen1] [Gen2] [Gen3]	Configure PEG 0:6:0 Max Speed
Max Link Width	<b>[Auto]</b> [Force X1] [Force X2] [Force X4] [Force X8]	Force PEG link to retrain to X1/2/4/8
Power Down Unused Lanes	[Disabled] <b>[Auto]</b>	Power Down Unused Lanes. Disabled: No power saving Auto: Bios will power down unused lanes based on the max possible link width
Gen3 Eq Phase 2	[Disabled] [Enabled] <b>[Auto]</b>	Perform Gen3 Equalization Phase 2
Gen3 Eq Phase 3 Method	<b>[Auto]</b> [Adaptive Hardware Equalization] [Adaptive Software Equalization] [Static Equalization] [Disabled]	Select Method for Gen3 Equalization Phase 3
ASPM	[Disabled] <b>[Auto]</b> [L0s] [L1] [L0sL1]	Control ASPM support for the PEG 3. This has no effect if PEG is not the currently active device.
ASPM L0s	[Root Port Only] [Endpoint Port Only] <b>[Both Root and Endpoint Ports]</b>	PEG3: Enable PCIe ASPM L0s.
De-emphasis Control	[-6dB] <b>[-3.5dB]</b>	PEG3: Configure the De-emphasis control on PEG
OBFF	[Disabled] <b>[Enabled]</b>	CPU PEG3 (0,6,0) OBFF Enable/Disable
LTR	[Disabled] <b>[Enabled]</b>	CPU PEG3 (0,6,0) Latency Reporting Enable/Disable

PEG3 Slot Power Limit Value	<b>minimum = 0</b> <b>maximum = 255</b> <b>step = 1</b> <b>default = 75</b>	Sets the upper limit on power supplied by slot. Power limit (in Watts) is calculated by multiplying this value by the Slot Power Limit Scale. Values 0-255
PEG3 Slot Power Limit Scale	<b>[1.0x]</b> [0.1x] [0.01x] [0.001x]	Select the scale used for the Slot Power Limit Value.
PEG3 Physical Slot Number	<b>minimum = 0</b> <b>maximum = 8191</b> <b>step = 1</b> <b>default = 3</b>	Set the physical slot number attached to this Port. The number has to be globally unique within the chassis. Values 0-8191
PEG3 Hotplug	<b>[Disabled]</b> [Enabled]	PCI Express Hot Plug Enable/Disable
Extra Bus Reserved (Except CFL)	<b>minimum = 0</b> <b>maximum = 7</b> <b>step = 1</b> <b>default = 0</b>	Extra Bus Reserved (0-7) for bridges behind this Root Bridge.
Reserved Memory (Except CFL)	<b>minimum = 1</b> <b>maximum = 20</b> <b>step = 1</b> <b>default = 10</b>	Reserved Memory for this Root Bridge (1-4096) MB
Reserved I/O (Except CFL)	<b>minimum = 4</b> <b>maximum = 20</b> <b>step = 4</b> <b>default = 4</b>	Reserved I/O (4K/8K/12K/16K/20K) Range for this Root Bridge.
PEG0 Max Payload size	<b>[Auto]</b> [128] [256]	Select PEG0 Max Payload Size; Choose Auto(Default Device Capability) or force to 128/256 Bytes
PEG1 Max Payload size	<b>[Auto]</b> [128] [256]	Select PEG1 Max Payload Size; Choose Auto(Default Device Capability) or force to 128/256 Bytes
PEG2 Max Payload size	<b>[Auto]</b> [128] [256]	Select PEG2 Max Payload Size; Choose Auto(Default Device Capability) or force to 128/256 Bytes
PEG3 Max Payload size	<b>[Auto]</b> [128] [256]	Select PEG3 Max Payload Size; Choose Auto(Default Device Capability) or force to 128/256 Bytes
Program PCIe ASPM after OpROM	<b>[Disabled]</b> [Enabled]	Enabled: PCIe ASPM will be programmed after OpROM. Disabled: PCIe ASPM will be programmed before OpROM.
Program Static Phase1 Eq	[Disabled] <b>[Enabled]</b>	Program Phase1 Presets/CTLEp
Gen3 Root Port Preset value for each Lane	(See Section 2.2.14.3.1)	Root Port preset value per lane for Gen3 Equalization
Gen3 Endpoint Preset value for each Lane	(See Section 2.2.14.3.2)	Endpoint preset value per lane for Gen3 Equalization. (Show as ProgramStaticPhase1Eq is Enable)

Gen3 Endpoint Hint value for each Lane	(See Section 2.2.14.3.3)	Endpoint Hint value per lane for Gen3 Equalization. (Show as ProgramStaticPhase1Eq is Enable)
Gen3 RxCTLE Control	(See Section 2.2.14.3.4)	Gen3 RxCTLE Control per Bundle.
Gen3 Adaptive Software Equalization		Gen3 Adaptive Software Equalization
Always Attempt SW EQ	<b>[Disabled]</b> [Enabled]	Always Attempt SW EQ, even it has been done once
Number of Presets to test	[7,3,5,8] [0 – 9] <b>[Auto]</b>	Choose between 7,3,5,8 and 0-9. Auto = current default (7,3,5,8) Do not change from the default unless debugging.
Allow PERST# GPIO Usage	[Disabled] <b>[Enabled]</b>	Enable/Disable GPIO-based resets to PEG endpoint(s) during margin search, if needed
SW EQ Enable VOC	[Jitter Only Test Mode] [Jitter & VOC Test Mode] <b>[Auto]</b>	Select Jitter & VOC test mode (default) or Jitter only test mode. Auto will current default (Enabled)
Jitter Dwell Time	<b>minimum = 0</b> <b>maximum = 65535</b> <b>step = 1</b> <b>default = 3000</b>	PEG Gen3 Preset Search dwell time [0..65535] in [usec]
Jitter Error Target	<b>minimum = 1</b> <b>maximum = 65535</b> <b>step = 1</b> <b>default = 2</b>	The margin search error target value [1..65535]
VOC Dwell Time	<b>minimum = 0</b> <b>maximum = 65535</b> <b>step = 1</b> <b>default = 10000</b>	The VOC margin search dwell time [0..65535] in [usec]
VOC Error Target	<b>minimum = 1</b> <b>maximum = 65535</b> <b>step = 1</b> <b>default = 2</b>	The VOC margin search error target value [1..65535]
Generate BDAT PEG Margin Data	<b>[Disabled]</b> [Generate Port Jitter Data]	Enable to generate BDAT PCIe margin tables
PEG IMR	<b>[Disabled]</b> [Enabled]	Enable/Disable PEG IMR PCIe IMR can either be enabled on the SA or PCH but not both simultaneously
PEG IMR Size	<b>minimum = 0</b> <b>maximum = 1024</b> <b>step = 1</b> <b>default = 0</b>	PEG Reserved Memory Size to be requested in MB. Maximum value of 1024 MB
RP index for IMR	<b>minimum = 1</b> <b>maximum = 4</b> <b>step = 1</b> <b>default = 1</b>	Selects which root port will be associated with IMR

PCIe Rx CEM Test Mode	<b>[Disabled]</b> [Enabled]	Enable/Disable PEG Rx CEM Loopback Mode
PEG Lane number for Test	<b>minimum = 0</b> <b>maximum = 15</b> <b>step = 1</b> <b>default = 0</b>	PEG Lane number for Rx CEM Loopback mode (0 ~ 15)
Non-Protocol Awareness	<b>[Disabled]</b> [Enabled]	Enable/Disable Non-Protocol Awareness
PCIe Spread Spectrum Clocking	[Disabled] <b>[Enabled]</b>	Allows disabling Spread Spectrum Clocking for compliance testing

### 2.2.15.3.1 Gen3 Root Port Preset value for each Lane

**Table 2-2-15-3-1. Gen3 Root Port Preset value for each Lane**

BIOS Setting	Options	Description
Gen3 Root Port Preset value for each Lane		
Lane 0	<b>minimum = 0</b> <b>maximum = 9</b> <b>step = 1</b> <b>default = 7</b>	Value for Lane 0
Lane 1	<b>minimum = 0</b> <b>maximum = 9</b> <b>step = 1</b> <b>default = 7</b>	Value for Lane 1
Lane 2	<b>minimum = 0</b> <b>maximum = 9</b> <b>step = 1</b> <b>default = 7</b>	Value for Lane 2
Lane 3	<b>minimum = 0</b> <b>maximum = 9</b> <b>step = 1</b> <b>default = 7</b>	Value for Lane 3
Lane 4	<b>minimum = 0</b> <b>maximum = 9</b> <b>step = 1</b> <b>default = 7</b>	Value for Lane 4
Lane 5	<b>minimum = 0</b> <b>maximum = 9</b> <b>step = 1</b> <b>default = 7</b>	Value for Lane 5
Lane 6	<b>minimum = 0</b> <b>maximum = 9</b> <b>step = 1</b> <b>default = 7</b>	Value for Lane 6
Lane 7	<b>minimum = 0</b> <b>maximum = 9</b> <b>step = 1</b>	Value for Lane 7

	<b>default = 7</b>	
Lane 8	<b>minimum = 0 maximum = 9 step = 1 default = 7</b>	Value for Lane 8
Lane 9	<b>minimum = 0 maximum = 9 step = 1 default = 7</b>	Value for Lane 9
Lane 10	<b>minimum = 0 maximum = 9 step = 1 default = 7</b>	Value for Lane 10
Lane 11	<b>minimum = 0 maximum = 9 step = 1 default = 7</b>	Value for Lane 11
Lane 12	<b>minimum = 0 maximum = 9 step = 1 default = 7</b>	Value for Lane 12
Lane 13	<b>minimum = 0 maximum = 9 step = 1 default = 7</b>	Value for Lane 13
Lane 14	<b>minimum = 0 maximum = 9 step = 1 default = 7</b>	Value for Lane 14
Lane 15	<b>minimum = 0 maximum = 9 step = 1 default = 7</b>	Value for Lane 15
Lane 16 (Except CFL)	<b>minimum = 0 maximum = 9 step = 1 default = 7</b>	Value for Lane 16
Lane 17 (Except CFL)	<b>minimum = 0 maximum = 9 step = 1 default = 7</b>	Value for Lane 17
Lane 18 (Except CFL)	<b>minimum = 0 maximum = 9 step = 1 default = 7</b>	Value for Lane 18
Lane 19 (Except CFL)	<b>minimum = 0 maximum = 9 step = 1</b>	Value for Lane 19

	<b>default = 7</b>	
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### 2.2.15.3.2 Gen3 Endpoint Preset value for each Lane

**Table 2-2-15-3-2. Gen3 Endpoint Preset value for each Lane**

BIOS Setting	Options	Description
Gen3 Endpoint Preset value for each Lane		
Lane 0	<b>minimum = 0 maximum = 9 step = 1 default = 7</b>	Value for Lane 0
Lane 1	<b>minimum = 0 maximum = 9 step = 1 default = 7</b>	Value for Lane 1
Lane 2	<b>minimum = 0 maximum = 9 step = 1 default = 7</b>	Value for Lane 2
Lane 3	<b>minimum = 0 maximum = 9 step = 1 default = 7</b>	Value for Lane 3
Lane 4	<b>minimum = 0 maximum = 9 step = 1 default = 7</b>	Value for Lane 4
Lane 5	<b>minimum = 0 maximum = 9 step = 1 default = 7</b>	Value for Lane 5
Lane 6	<b>minimum = 0 maximum = 9 step = 1 default = 7</b>	Value for Lane 6
Lane 7	<b>minimum = 0 maximum = 9 step = 1 default = 7</b>	Value for Lane 7
Lane 8	<b>minimum = 0 maximum = 9 step = 1 default = 7</b>	Value for Lane 8
Lane 9	<b>minimum = 0 maximum = 9 step = 1 default = 7</b>	Value for Lane 9

Lane 10	<b>minimum = 0</b> <b>maximum = 9</b> <b>step = 1</b> <b>default = 7</b>	Value for Lane 10
Lane 11	<b>minimum = 0</b> <b>maximum = 9</b> <b>step = 1</b> <b>default = 7</b>	Value for Lane 11
Lane 12	<b>minimum = 0</b> <b>maximum = 9</b> <b>step = 1</b> <b>default = 7</b>	Value for Lane 12
Lane 13	<b>minimum = 0</b> <b>maximum = 9</b> <b>step = 1</b> <b>default = 7</b>	Value for Lane 13
Lane 14	<b>minimum = 0</b> <b>maximum = 9</b> <b>step = 1</b> <b>default = 7</b>	Value for Lane 14
Lane 15	<b>minimum = 0</b> <b>maximum = 9</b> <b>step = 1</b> <b>default = 7</b>	Value for Lane 15
Lane 16 (Except CFL)	<b>minimum = 0</b> <b>maximum = 9</b> <b>step = 1</b> <b>default = 7</b>	Value for Lane 16
Lane 17 (Except CFL)	<b>minimum = 0</b> <b>maximum = 9</b> <b>step = 1</b> <b>default = 7</b>	Value for Lane 17
Lane 18 (Except CFL)	<b>minimum = 0</b> <b>maximum = 9</b> <b>step = 1</b> <b>default = 7</b>	Value for Lane 18
Lane 19 (Except CFL)	<b>minimum = 0</b> <b>maximum = 9</b> <b>step = 1</b> <b>default = 7</b>	Value for Lane 19

### 2.2.15.3.3 Gen3 Endpoint Hint value for each Lane

**Table 2-2-15-3-3. Gen3 Endpoint Hint value for each Lane**

BIOS Setting	Options	Description
Gen3 Endpoint Hint value for each Lane		
Lane 0	<b>minimum = 0</b> <b>maximum = 6</b>	Value for Lane 0

	<b>step = 1</b> <b>default = 2</b>	
Lane 1	<b>minimum = 0</b> <b>maximum = 6</b> <b>step = 1</b> <b>default = 2</b>	Value for Lane 1
Lane 2	<b>minimum = 0</b> <b>maximum = 6</b> <b>step = 1</b> <b>default = 2</b>	Value for Lane 2
Lane 3	<b>minimum = 0</b> <b>maximum = 6</b> <b>step = 1</b> <b>default = 2</b>	Value for Lane 3
Lane 4	<b>minimum = 0</b> <b>maximum = 6</b> <b>step = 1</b> <b>default = 2</b>	Value for Lane 4
Lane 5	<b>minimum = 0</b> <b>maximum = 6</b> <b>step = 1</b> <b>default = 2</b>	Value for Lane 5
Lane 6	<b>minimum = 0</b> <b>maximum = 6</b> <b>step = 1</b> <b>default = 2</b>	Value for Lane 6
Lane 7	<b>minimum = 0</b> <b>maximum = 6</b> <b>step = 1</b> <b>default = 2</b>	Value for Lane 7
Lane 8	<b>minimum = 0</b> <b>maximum = 6</b> <b>step = 1</b> <b>default = 2</b>	Value for Lane 8
Lane 9	<b>minimum = 0</b> <b>maximum = 6</b> <b>step = 1</b> <b>default = 2</b>	Value for Lane 9
Lane 10	<b>minimum = 0</b> <b>maximum = 6</b> <b>step = 1</b> <b>default = 2</b>	Value for Lane 10
Lane 11	<b>minimum = 0</b> <b>maximum = 6</b> <b>step = 1</b> <b>default = 2</b>	Value for Lane 11
Lane 12	<b>minimum = 0</b> <b>maximum = 6</b> <b>step = 1</b>	Value for Lane 12

	<b>default = 2</b>	
Lane 13	<b>minimum = 0 maximum = 6 step = 1 default = 2</b>	Value for Lane 13
Lane 14	<b>minimum = 0 maximum = 6 step = 1 default = 2</b>	Value for Lane 14
Lane 15	<b>minimum = 0 maximum = 6 step = 1 default = 2</b>	Value for Lane 15
Lane 16 (Except CFL)	<b>minimum = 0 maximum = 6 step = 1 default = 2</b>	Value for Lane 16
Lane 17 (Except CFL)	<b>minimum = 0 maximum = 6 step = 1 default = 2</b>	Value for Lane 17
Lane 18 (Except CFL)	<b>minimum = 0 maximum = 6 step = 1 default = 2</b>	Value for Lane 18
Lane 19 (Except CFL)	<b>minimum = 0 maximum = 6 step = 1 default = 2</b>	Value for Lane 19

### 2.2.15.3.4 Gen3 RxCTLE Control

**Table 2-2-15-3-4. Gen3 RxCTLE Control**

BIOS Setting	Options	Description
Gen3 RxCTLE Control		
Bundle0	<b>minimum = 0 maximum = 15 step = 1 default = 0</b>	Gen3 RxCTLE setting for Bundle0 (Lane0, Lane1)
Bundle1	<b>minimum = 0 maximum = 15 step = 1 default = 0</b>	Gen3 RxCTLE setting for Bundle1 (Lane2, Lane3)
Bundle2	<b>minimum = 0 maximum = 15 step = 1 default = 0</b>	Gen3 RxCTLE setting for Bundle2 (Lane4, Lane5)

Bundle3	<b>minimum = 0</b> <b>maximum = 15</b> <b>step = 1</b> <b>default = 0</b>	Gen3 RxCTLE setting for Bundle3 (Lane6, Lane7)
Bundle4	<b>minimum = 0</b> <b>maximum = 15</b> <b>step = 1</b> <b>default = 0</b>	Gen3 RxCTLE setting for Bundle4 (Lane8, Lane9)
Bundle5	<b>minimum = 0</b> <b>maximum = 15</b> <b>step = 1</b> <b>default = 0</b>	Gen3 RxCTLE setting for Bundle5 (Lane10, Lane11)
Bundle6	<b>minimum = 0</b> <b>maximum = 15</b> <b>step = 1</b> <b>default = 0</b>	Gen3 RxCTLE setting for Bundle6 (Lane12, Lane13)
Bundle7	<b>minimum = 0</b> <b>maximum = 15</b> <b>step = 1</b> <b>default = 0</b>	Gen3 RxCTLE setting for Bundle7 (Lane14, Lane15)
Bundle8 (Except CFL)	<b>minimum = 0</b> <b>maximum = 15</b> <b>step = 1</b> <b>default = 0</b>	Gen3 RxCTLE setting for Bundle8 (Lane16, Lane17)
Bundle9 (Except CFL)	<b>minimum = 0</b> <b>maximum = 15</b> <b>step = 1</b> <b>default = 0</b>	Gen3 RxCTLE setting for Bundle9 (Lane18, Lane19)
PEG10 RxCTLE Override	<b>[Disabled]</b> [Enabled]	When Enabled, it overrides PEG0 RxCTLE adaptive behavior
PEG11 RxCTLE Override	<b>[Disabled]</b> [Enabled]	When Enabled, it overrides PEG1 RxCTLE adaptive behavior
PEG12 RxCTLE Override	<b>[Disabled]</b> [Enabled]	When Enabled, it overrides PEG2 RxCTLE adaptive behavior
PEG60 RxCTLE Override	<b>[Disabled]</b> [Enabled]	When Enabled, it overrides PEG3 RxCTLE adaptive behavior
DMI RxCTLE Override	<b>[Disabled]</b> [Enabled]	When Enabled, it overrides DMI RxCTLE adaptive behavior

### 2.2.15.4 TCSS setup menu

**Table 2-2-15-4. TCSS setup menu**

BIOS Setting	Options	Description
TCSS Configuration		
IOM FW version:	No Options	

PHY FW version:	No Options	
TBT FW IMR Status:	No Options	
TBT FW version:	No Options	
Deepest TC state:	No Options	
TCSS xHCI Support	[Disabled] <b>[Enable]</b>	Enable/Disable TCSS xHCI
TCSS USB Configuration	(See Section 2.2.15.4.1)	SA TCSS USB Configuration settings
ITBT PCIE0 Root Port	[Disabled] <b>[Enable]</b>	Enable/Disable ITBT PCIE ROOT
ITBT PCIE1 Root Port	[Disabled] <b>[Enable]</b>	Enable/Disable ITBT PCIE ROOT
ITBT PCIE2 Root Port	[Disabled] <b>[Enable]</b>	Enable/Disable ITBT PCIE ROOT
ITBT PCIE3 Root Port	[Disabled] <b>[Enable]</b>	Enable/Disable ITBT PCIE ROOT
ITBT DMA0	[Disabled] <b>[Enable]</b>	Enable/Disable ITBT DMA0
ITBT DMA1	[Disabled] <b>[Enable]</b>	Enable/Disable ITBT DMA1
VCCST status of IOM	[Disabled] <b>[Enable]</b>	Enables/Disables VCCST. \nEnable: Sends VCCST ON message to EC or PMC \nDisable: Sends VCCST OFF message to EC or PMC
D3 Cold Enable/Disable	[Disabled] <b>[Enable]</b>	Enables/Disables D3 Cold. \nEnable: D3 cold support for IOM is enabled \nDisable: D3 cold support for IOM is Disabled
D3 Hot Enable/Disable	[Disabled] <b>[Enable]</b>	Enables/Disables D3 Hot. \nEnable: D3 Hot support for IOM is enabled \nDisable: D3 Hot support for IOM is Disabled
Tc C-State Limit	[Disabled] [1] [2] [4] [5] [6] [7] <b>[10]</b>	BIOS mailbox to limit deepest TCx state
PCI Express Root Port 0	(See Section 2.2.15.4.2)	PCI Express Root Port Settings.
PCI Express Root Port 1	(See Section 2.2.15.4.3)	PCI Express Root Port Settings.
PCI Express Root Port 2	(See Section 2.2.15.4.4)	PCI Express Root Port Settings.
PCI Express Root Port 3	(See Section 2.2.15.4.5)	PCI Express Root Port Settings.

### 2.2.15.4.1 TCSS USB Configuration

**Table 2-2-15-4-1. TCSS USB Configuration**

BIOS Setting	Options	Description
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TCSS USB Configuration		
USB CONNECT OVERRIDE	<b>[Disabled]</b> [Enabled]	Option will allow VCCSTTPC to turn off even when there is a connection for a USB3 port.
TCSS xDCI Support	<b>[Disabled]</b> [Enabled]	Enable/Disable TCSS xDCI
TCSS CPU USB PDO Programming	[Disabled] <b>[Enable]</b>	Select 'Enabled' if Port Disable Override functionality is used. <i>(Below will show at this option set Enable)</i>
TCSS CPU USB Port Disable Override	[Disabled] <b>[Select Per-Pin]</b>	Selectively Enable/Disable the corresponding USB port from reporting a Device Connection to the controller. <i>(Below will show at this option set Select Per-Pin)</i>
TCSS CPU USB SS Physical Connector #0	[Disabled] <b>[Enable]</b>	Enable/Disable this TCSS CPU USB Physical Connector (physical port). Once disabled, any USB devices plug into the connector will not be detected by BIOS or OS.
TCSS CPU USB SS Physical Connector #1	[Disabled] <b>[Enable]</b>	Enable/Disable this TCSS CPU USB Physical Connector (physical port). Once disabled, any USB devices plug into the connector will not be detected by BIOS or OS.
TCSS CPU USB SS Physical Connector #2	[Disabled] <b>[Enable]</b>	Enable/Disable this TCSS CPU USB Physical Connector (physical port). Once disabled, any USB devices plug into the connector will not be detected by BIOS or OS.
TCSS CPU USB SS Physical Connector #3	[Disabled] <b>[Enable]</b>	Enable/Disable this TCSS CPU USB Physical Connector (physical port). Once disabled, any USB devices plug into the connector will not be detected by BIOS or OS.

#### 2.2.15.4.2 PCI Express Root Port 0

**Table 2-2-15-4-2. PCI Express Root Port 0**

BIOS Setting	Options	Description
PCI Express Root Port 0		
PTM	[Disabled] <b>[Enable]</b>	Enable/Disable Precision Time Measurement
SA PCIe LTR Configuration	No Options	None
LTR	[Disabled] <b>[Enable]</b>	PCIE Latency Reporting Enable/Disable

Snoop Latency Override	[Disabled] <b>[Enable]</b>	Snoop Latency Override for SA PCIE. \nDisabled: Disable override. \nManual: Manually enter override values. \nAuto (default): Maintain default BIOS flow.
Snoop Latency Value	<b>default = 200</b>	LTR Snoop Latency value of SA PCIE
Snoop Latency Multiplier	[1ns] [32ns] <b>[1024ns]</b> [32768ns] [1048576ns] [33554432ns]	LTR Snoop Latency Multiplier of SA PCIE
Non Snoop Latency Override	[Disabled] <b>[Enable]</b>	Non Snoop Latency Override for SA PCIE. \nDisabled: Disable override. \nManual: Manually enter override values. \nAuto (default): Maintain default BIOS flow.
Non Snoop Latency Value	<b>default = 200</b>	LTR Non Snoop Latency value of SA PCIE
Non Snoop Latency Multiplier	[1ns] [32ns] <b>[1024ns]</b> [32768ns] [1048576ns] [33554432ns]	LTR Non Snoop Latency Multiplier of SA PCIE
Force LTR Override	<b>[Disabled]</b> [Enabled]	Force LTR Override for ITBT PCIE. \nDisabled: LTR override values will not be forced. \nEnable: LTR override values will be forced and LTR messages from the device will be ignored.
LTR Lock	<b>[Disabled]</b> [Enabled]	PCIE LTR Configuration Lock

### 2.2.15.4.3 PCI Express Root Port 1

**Table 2-2-15-4-3. PCI Express Root Port 1**

BIOS Setting	Options	Description
PCI Express Root Port 1		
PTM	[Disabled] <b>[Enable]</b>	Enable/Disable Precision Time Measurement
SA PCIe LTR Configuration	No Options	None
LTR	[Disabled] <b>[Enable]</b>	PCIE Latency Reporting Enable/Disable
Snoop Latency Override	[Disabled] <b>[Enable]</b>	Snoop Latency Override for SA PCIE. \nDisabled: Disable override. \nManual: Manually enter override values. \nAuto (default): Maintain default BIOS flow.
Snoop Latency Value	<b>default = 200</b>	LTR Snoop Latency value of SA PCIE

Snoop Latency Multiplier	[1ns] [32ns] <b>[1024ns]</b> [32768ns] [1048576ns] [33554432ns]	LTR Snoop Latency Multiplier of SA PCIE
Non Snoop Latency Override	[Disabled] <b>[Enable]</b>	Non Snoop Latency Override for SA PCIE.\nDisabled: Disable override.\nManual: Manually enter override values.\nAuto (default): Maintain default BIOS flow.
Non Snoop Latency Value	<b>default = 200</b>	LTR Non Snoop Latency value of SA PCIE
Non Snoop Latency Multiplier	[1ns] [32ns] <b>[1024ns]</b> [32768ns] [1048576ns] [33554432ns]	LTR Non Snoop Latency Multiplier of SA PCIE
Force LTR Override	<b>[Disabled]</b> [Enabled]	Force LTR Override for ITBT PCIE.\nDisabled: LTR override values will not be forced.\nEnable: LTR override values will be forced and LTR messages from the device will be ignored.
LTR Lock	<b>[Disabled]</b> [Enabled]	PCIE LTR Configuration Lock

### 2.2.15.4.3 PCI Express Root Port 2

**Table 2-2-15-4-3. PCI Express Root Port 2**

BIOS Setting	Options	Description
PCI Express Root Port 2		
PTM	[Disabled] <b>[Enable]</b>	Enable/Disable Precision Time Measurement
SA PCIe LTR Configuration	No Options	None
LTR	[Disabled] <b>[Enable]</b>	PCIE Latency Reporting Enable/Disable
Snoop Latency Override	[Disabled] <b>[Enable]</b>	Snoop Latency Override for SA PCIE.\nDisabled: Disable override.\nManual: Manually enter override values.\nAuto (default): Maintain default BIOS flow.
Snoop Latency Value	<b>default = 200</b>	LTR Snoop Latency value of SA PCIE
Snoop Latency Multiplier	[1ns] [32ns] <b>[1024ns]</b> [32768ns] [1048576ns] [33554432ns]	LTR Snoop Latency Multiplier of SA PCIE
Non Snoop Latency Override	[Disabled] <b>[Enable]</b>	Non Snoop Latency Override for SA PCIE.\nDisabled: Disable override.\nManual: Manually enter override values.\nAuto (default): Maintain default BIOS flow.

Non Snoop Latency Value	<b>default = 200</b>	LTR Non Snoop Latency value of SA PCIE
Non Snoop Latency Multiplier	[1ns] [32ns] <b>[1024ns]</b> [32768ns] [1048576ns] [33554432ns]	LTR Non Snoop Latency Multiplier of SA PCIE
Force LTR Override	<b>[Disabled]</b> [Enabled]	Force LTR Override for ITBT PCIE. Disabled: LTR override values will not be forced. Enable: LTR override values will be forced and LTR messages from the device will be ignored.
LTR Lock	<b>[Disabled]</b> [Enabled]	PCIE LTR Configuration Lock

### 2.2.15.4.4 PCI Express Root Port 3

**Table 2-2-15-4-4. PCI Express Root Port 3**

BIOS Setting	Options	Description
PCI Express Root Port 3		
PTM	[Disabled] <b>[Enable]</b>	Enable/Disable Precision Time Measurement
SA PCIe LTR Configuration	No Options	None
LTR	[Disabled] <b>[Enable]</b>	PCIE Latency Reporting Enable/Disable
Snoop Latency Override	[Disabled] <b>[Enable]</b>	Snoop Latency Override for SA PCIE. Disabled: Disable override. Manual: Manually enter override values. Auto (default): Maintain default BIOS flow.
Snoop Latency Value	<b>default = 200</b>	LTR Snoop Latency value of SA PCIE
Snoop Latency Multiplier	[1ns] [32ns] <b>[1024ns]</b> [32768ns] [1048576ns] [33554432ns]	LTR Snoop Latency Multiplier of SA PCIE
Non Snoop Latency Override	[Disabled] <b>[Enable]</b>	Non Snoop Latency Override for SA PCIE. Disabled: Disable override. Manual: Manually enter override values. Auto (default): Maintain default BIOS flow.
Non Snoop Latency Value	<b>default = 200</b>	LTR Non Snoop Latency value of SA PCIE
Non Snoop Latency Multiplier	[1ns] [32ns] <b>[1024ns]</b> [32768ns] [1048576ns] [33554432ns]	LTR Non Snoop Latency Multiplier of SA PCIE
Force LTR Override	<b>[Disabled]</b> [Enabled]	Force LTR Override for ITBT PCIE. Disabled: LTR override

		values will not be forced.\nEnable: LTR override values will be forced and LTR messages from the device will be ignored.
LTR Lock	<b>[Disabled] [Enabled]</b>	PCIE LTR Configuration Lock

### 2.2.15.5 VMD setup menu

**Table 2-2-15-5. VMD setup menu**

BIOS Setting	Options	Description
VMD setup menu		
Enable VMD controller	[Disabled] <b>[Enabled]</b>	Enable/Disable to VMD controller <i>(Below will show at this option set Enable)</i>
Enable VMD Global Mapping	[Disabled] <b>[Enabled]</b>	Enable/Disable to VMD Global Mapping
RAID0	[Disabled] <b>[Enabled]</b>	Enable/Disable RAID0 support
RAID1	[Disabled] <b>[Enabled]</b>	Enable/Disable RAID1 support
RAID5	[Disabled] <b>[Enabled]</b>	Enable/Disable RAID5 support
RAID10	[Disabled] <b>[Enabled]</b>	Enable/Disable RAID10 support
Intel Rapid Recovery Technology	[Disabled] <b>[Enabled]</b>	Enable/Disable Intel Rapid Recovery Technology.
RRT volumes can span internal and eSATA drives	[Disabled] <b>[Enabled]</b>	Enable/Disable RRT volumes can span internal and eSATA drives.
Intel(R) Optane(TM) Memory	[Disabled] <b>[Enabled]</b>	Enable/Disable System Acceleration with Intel(R) Optane(TM) Memory feature.

### 2.2.15.6 Display setup menu

**Table 2-2-15-6 Display setup menu**

BIOS Setting	Options	Description
Display Configuration		

### 2.2.15.7 PCI Express Configuration

**Table 2-2-15-7. PCI Express Configuration**

BIOS Setting	Options	Description
PCI Express Configuration		

Fia Programming	[Disabled] <b>[Enable]</b>	<i>Load Fia Configuration if Enabled for each root port.</i>
Compliance Test Mode	<b>[Disabled]</b> [Enabled]	Enable when using Compliance Load Board
CDR Relock	[Disabled] <b>[Enable]</b>	CDR Relock for CPU DMI
Assertion on Link Down GPIOs	<b>[Disabled]</b> [Enabled]	GPIO Assertion on Link Down
PCI Express Slot Selection	<b>[M2 slot]</b> [CEMx4 slot]	Select the PCIe M2 or CEMx4 slot
PCI Express Root Port 1	(See Section 2.2.15.7.1)	PCI Express Root Port Settings.
PCI Express Root Port 2	(See Section 2.2.15.7.2)	PCI Express Root Port Settings.
PCI Express Root Port 3	(See Section 2.2.15.7.3)	PCI Express Root Port Settings.

### 2.2.15.8 MIPI Camera Configuration

**Table 2-2-15-8. MIPI Camera Configuration**

BIOS Setting	Options	Description
CVF Support	[Native Ios] [Disabled] <b>[USB Bridge]</b>	Disables/Enables CVF using either Native IOs or USB IOs Expansion.
Control Logic 1	[Disabled] <b>[Enable]</b>	Control Logic 1 (Below option will show at this option set Enabled)
Control Logic options	(See Section 2.2.15.8.1)	Control Logic options
Control Logic 2	<b>[Disabled]</b> [Enabled]	Control Logic 2 (Below option will show at this option set Enabled)
Control Logic options	(See Section 2.2.15.8.2)	Control Logic options
Control Logic 3	<b>[Disabled]</b> [Enabled]	Control Logic 3 (Below option will show at this option set Enabled)
Control Logic options	(See Section 2.2.15.8.3)	Control Logic options
Control Logic 4	<b>[Disabled]</b> [Enabled]	Control Logic 4 (Below option will show at this option set Enabled)
Control Logic options	(See Section 2.2.15.8.4)	Control Logic options
Camera1	[Disabled] <b>[Enable]</b>	Camera1 (Below option will show at this option set Enabled)
Link options	(See Section 2.2.15.8.5)	Link options

Camera2	[Disabled] <b>[Enable]</b>	Camera2 (Below option will show at this option set Enabled)
Link options	(See Section 2.2.15.8.6)	Link options
Flash options	(See Section 2.2.15.8.7)	Flash options
Camera3	<b>[Disabled]</b> [Enabled]	Camera3 (Below option will show at this option set Enabled)
Link options	(See Section 2.2.15.8.8)	Link options
Camera4	<b>[Disabled]</b> [Enabled]	Camera1 (Below option will show at this option set Enabled)
Link options	(See Section 2.2.15.8.9)	Link options

### 2.2.15.8.1 Control Logic options

**Table 2-2-15-8-1. Control Logic options**

BIOS Setting	Options	Description
Control Logic options		
Control Logic Type	<b>[Discrete]</b> [PMIC_TPS68470] [PMIC_UP6641] [PMIC_USER0] [PMIC_USER1]	Control Logic Type
CRD Version	[PTC] [CRD-D] <b>[CRD-G]</b> [Kilshon-PPV] [CRD-G2]	CRD Version
Input Clock	[20 MHz] [24 MHz] [26 MHz] <b>[19.2 MHz]</b>	Input Clock
PCH Clock Source	<b>[IMGCLKOUT_0]</b> [IMGCLKOUT_1]	This option specifies which IMGCLKOUT is chosen (This option will show at Control Logic Type set Discrete or Control Logic Type set PMIC_TPS68470 and CRD Version set CRD-G3)
PMIC Flash Panel	[Front] <b>[Back]</b>	PMIC Flash Panel (This option will show at CRD Version set CRD-G or CRD-G2)
(Below options will show at Control Logic Type set PMIC_TPS68470 or PMIC_UP6641 or PMIC_USER0 or PMIC_USER1)		
I2C Channel	[I2C0] [I2C1] [I2C2] <b>[I2C3]</b> [I2C4] [I2C5]	I2C Channel
I2C Address	<b>minimum = 0</b> <b>maximum = 0x7F</b> <b>step = 1</b>	I2C Address

	<b>default = 0x4D</b>	
<u>(Below options will show at Control Logic Type set PMIC TPS68470 or PMIC UP6641)</u>		
WLED1 Type	[Disabled] <b>[White Led]</b> [Warm Led] [IR Led] [Xeon Led]	WLED Type
WLED1 Flash Max Current	<b>minimum = 0</b> <b>maximum = 0x1F</b> <b>step = 1</b> <b>default = 0</b>	WLED Flash Max Current Valid range is 0x00-0x1F 0x00 for HW default max current
WLED1 Torch Max Current	<b>minimum = 0</b> <b>maximum = 0x7</b> <b>step = 1</b> <b>default = 0</b>	WLED Torch Max Current Valid range is 0x00-0x07 0x00 for HW default max current
WLED2 Type	[Disabled] [White Led] [Warm Led] <b>[IR Led]</b> [Xeon Led]	WLED Type
WLED2 Flash Max Current	<b>minimum = 0</b> <b>maximum = 0x1F</b> <b>step = 1</b> <b>default = 0</b>	WLED Flash Max Current Valid range is 0x00-0x1F 0x00 for HW default max current
WLED2 Torch Max Current	<b>minimum = 0</b> <b>maximum = 0x7</b> <b>step = 1</b> <b>default = 0</b>	WLED Torch Max Current Valid range is 0x00-0x07 0x00 for HW default max current
SubPlatformId	<b>minimum = 0</b> <b>maximum = 0xF</b> <b>step = 1</b> <b>default = 0</b>	SubPlatformId
<u>(Below options will show at Control Logic Type set Discrete or PMIC TPS68470 or PMIC UP6641)</u>		
Number of GPIO Pins	<b>minimum = 0</b> <b>maximum = 4</b> <b>step = 1</b> <b>default = 0</b>	Number of GPIO Pins
<u>(Below options will show at Number of GPIO Pins set 1 or 2 or 3 or 4)</u>		
GPIO 0		
Group Pad Number	<b>minimum = 0</b> <b>maximum = 23</b> <b>step = 1</b> <b>default = 22</b>	Group Pad Number
Group Number	[A] [B] [C] <b>[D]</b> [E] [F] [G] [H]	Group Number
Function	<b>[Reset]</b> [Power_En] [Clock_En] [pLED_En]	Function
Active Value	<b>minimum = 0</b> <b>maximum = 1</b> <b>step = 1</b> <b>default = 1</b>	Active Value

Initial Value	<b>minimum = 0</b> <b>maximum = 1</b> <b>step = 1</b> <b>default = 0</b>	Initial Value
(Below options will show at Number of GPIO Pins set 2 or 3 or 4)		
GPIO 1		
Group Pad Number	<b>minimum = 0</b> <b>maximum = 23</b> <b>step = 1</b> <b>default = 11</b>	Group Pad Number
Group Number	[A] [B] [C] <b>[D]</b> [E] [F] [G] [H]	Group Number
Function	<b>[Reset]</b> [Power_En] [Clock_En] [pLED_En]	Function
Active Value	<b>minimum = 0</b> <b>maximum = 1</b> <b>step = 1</b> <b>default = 1</b>	Active Value
Initial Value	<b>minimum = 0</b> <b>maximum = 1</b> <b>step = 1</b> <b>default = 0</b>	Initial Value
(Below options will show at Number of GPIO Pins set 3 or 4)		
GPIO 2		
Group Pad Number	<b>minimum = 0</b> <b>maximum = 23</b> <b>step = 1</b> <b>default = 11</b>	Group Pad Number
Group Number	[A] [B] [C] <b>[D]</b> [E] [F] [G] [H]	Group Number
Function	[Reset] [Power_En] <b>[Clock_En]</b> [pLED_En]	Function
Active Value	<b>minimum = 0</b> <b>maximum = 1</b> <b>step = 1</b> <b>default = 1</b>	Active Value
Initial Value	<b>minimum = 0</b> <b>maximum = 1</b> <b>step = 1</b> <b>default = 0</b>	Initial Value
(Below options will show at Number of GPIO Pins set 4)		
GPIO 3		
Group Pad Number	<b>minimum = 0</b> <b>maximum = 23</b>	Group Pad Number

	<b>step = 1</b> <b>default = 11</b>	
Group Number	[A] [B] [C] <b>[D]</b> [E] [F] [G] [H]	Group Number
Function	<b>[Reset]</b> [Power_En] [Clock_En] [pLED_En]	Function
Active Value	<b>minimum = 0</b> <b>maximum = 1</b> <b>step = 1</b> <b>default = 1</b>	Active Value
Initial Value	<b>minimum = 0</b> <b>maximum = 1</b> <b>step = 1</b> <b>default = 0</b>	Initial Value

### 2.2.15.8.2 Control Logic options

**Table 2-2-15-8-2. Control Logic options**

BIOS Setting	Options	Description
Control Logic options		
Control Logic Type	<b>[Discrete]</b> [PMIC_TPS68470] [PMIC_UP6641] [PMIC_USER0] [PMIC_USER1]	Control Logic Type
CRD Version	[PTC] <b>[CRD-D]</b> [CRD-G] [Kilshon-PPV] [CRD-G2]	CRD Version
Input Clock	<b>[20 MHz]</b> [24 MHz] [26 MHz] [19.2 MHz]	Input Clock
PCH Clock Source	[IMGCLKOUT_0] <b>[IMGCLKOUT_1]</b>	This option specifies which IMGCLKOUT is chosen (This option will show at Control Logic Type set Discrete or Control Logic Type set PMIC TPS68470 and CRD Version set CRD-G3)
PMIC Flash Panel	[Front] <b>[Back]</b>	PMIC Flash Panel (This option will show at CRD Version set CRD-G or CRD-G2)
<u>(Below options will show at Control Logic Type set PMIC TPS68470 or PMIC UP6641 or PMIC_USER0 or PMIC_USER1)</u>		
I2C Channel	[I2C0] [I2C1] [I2C2] <b>[I2C3]</b> [I2C4] [I2C5]	I2C Channel
I2C Address	<b>minimum = 0</b> <b>maximum = 0x7F</b> <b>step = 1</b> <b>default = 0x49</b>	I2C Address

<u>(Below options will show at Control Logic Type set PMIC_TPS68470 or PMIC_UP6641)</u>		
WLED1 Type	<b>[Disabled]</b> [White Led] [Warm Led] [IR Led] [Xeon Led]	WLED Type
WLED1 Flash Max Current	<b>minimum = 0</b> <b>maximum = 0x1F</b> <b>step = 1</b> <b>default = 0</b>	WLED Flash Max Current Valid range is 0x00-0x1F 0x00 for HW default max current
WLED1 Torch Max Current	<b>minimum = 0</b> <b>maximum = 0x7</b> <b>step = 1</b> <b>default = 0</b>	WLED Torch Max Current Valid range is 0x00-0x07 0x00 for HW default max current
WLED2 Type	<b>[Disabled]</b> [White Led] [Warm Led] [IR Led] [Xeon Led]	WLED Type
WLED2 Flash Max Current	<b>minimum = 0</b> <b>maximum = 0x1F</b> <b>step = 1</b> <b>default = 0</b>	WLED Flash Max Current Valid range is 0x00-0x1F 0x00 for HW default max current
WLED2 Torch Max Current	<b>minimum = 0</b> <b>maximum = 0x7</b> <b>step = 1</b> <b>default = 0</b>	WLED Torch Max Current Valid range is 0x00-0x07 0x00 for HW default max current
SubPlatformId	<b>minimum = 0</b> <b>maximum = 0xF</b> <b>step = 1</b> <b>default = 0</b>	SubPlatformId
<u>(Below options will show at Control Logic Type set Discrete or PMIC_TPS68470 or PMIC_UP6641)</u>		
Number of GPIO Pins	<b>minimum = 0</b> <b>maximum = 4</b> <b>step = 1</b> <b>default = 2</b>	Number of GPIO Pins
<u>(Below options will show at Number of GPIO Pins set 1 or 2 or 3 or 4)</u>		
GPIO 0		
Group Pad Number	<b>minimum = 0</b> <b>maximum = 23</b> <b>step = 1</b> <b>default = 22</b>	Group Pad Number
Group Number	[A] [B] [C] [D] [E] [F] [G] <b>[H]</b>	Group Number
Function	<b>[Reset]</b> [Power_En] [Clock_En] [pLED_En]	Function
Active Value	<b>minimum = 0</b> <b>maximum = 1</b> <b>step = 1</b> <b>default = 1</b>	Active Value

Initial Value	<b>minimum = 0</b> <b>maximum = 1</b> <b>step = 1</b> <b>default = 0</b>	Initial Value
<u>(Below options will show at Number of GPIO Pins set 2 or 3 or 4)</u>		
GPIO 1		
Group Pad Number	<b>minimum = 0</b> <b>maximum = 23</b> <b>step = 1</b> <b>default = 16</b>	Group Pad Number
Group Number	[A] [B] [C] [D] [E] [F] [G] [H]	Group Number
Function	[Reset] [Power_En] [Clock_En] [pLED_En]	Function
Active Value	<b>minimum = 0</b> <b>maximum = 1</b> <b>step = 1</b> <b>default = 1</b>	Active Value
Initial Value	<b>minimum = 0</b> <b>maximum = 1</b> <b>step = 1</b> <b>default = 0</b>	Initial Value
<u>(Below options will show at Number of GPIO Pins set 3 or 4)</u>		
GPIO 2		
Group Pad Number	<b>minimum = 0</b> <b>maximum = 23</b> <b>step = 1</b> <b>default = 11</b>	Group Pad Number
Group Number	[A] [B] [C] [D] [E] [F] [G] [H]	Group Number
Function	[Reset] [Power_En] [Clock_En] [pLED_En]	Function
Active Value	<b>minimum = 0</b> <b>maximum = 1</b> <b>step = 1</b> <b>default = 1</b>	Active Value
Initial Value	<b>minimum = 0</b> <b>maximum = 1</b> <b>step = 1</b> <b>default = 0</b>	Initial Value
<u>(Below options will show at Number of GPIO Pins set 4)</u>		
GPIO 3		
Group Pad Number	<b>minimum = 0</b> <b>maximum = 23</b>	Group Pad Number

	<b>step = 1</b> <b>default = 11</b>	
Group Number	[A] [B] [C] [ <b>D</b> ] [E] [F] [G] [H]	Group Number
Function	[ <b>Reset</b> ] [Power_En] [Clock_En] [pLED_En]	Function
Active Value	<b>minimum = 0</b> <b>maximum = 1</b> <b>step = 1</b> <b>default = 1</b>	Active Value
Initial Value	<b>minimum = 0</b> <b>maximum = 1</b> <b>step = 1</b> <b>default = 0</b>	Initial Value

### 2.2.15.8.3 Control Logic options

**Table 2-2-15-8-3. Control Logic options**

BIOS Setting	Options	Description
Control Logic options		
Control Logic Type	[Discrete] [ <b>PMIC_TPS68470</b> ] [PMIC_UP6641] [PMIC_USER0] [PMIC_USER1]	Control Logic Type
CRD Version	[PTC] [CRD-D] [CRD-G] [Kilshon-PPV] [ <b>CRD-G2</b> ]	CRD Version
Input Clock	[ <b>20 MHz</b> ] [24 MHz] [26 MHz] [19.2 MHz]	Input Clock
PCH Clock Source	[ <b>IMGCLKOUT_0</b> ] [IMGCLKOUT_1]	This option specifies which IMGCLKOUT is chosen (This option will show at Control Logic Type set Discrete or Control Logic Type set PMIC_TPS68470 and CRD Version set CRD-G3)
PMIC Flash Panel	[Front] [ <b>Back</b> ]	PMIC Flash Panel (This option will show at CRD Version set CRD-G or CRD-G2)
(Below options will show at Control Logic Type set PMIC_TPS68470 or PMIC_UP6641 or PMIC_USER0 or PMIC_USER1)		
I2C Channel	[I2C0] [I2C1] [ <b>I2C2</b> ] [I2C3] [I2C4] [I2C5]	I2C Channel
I2C Address	<b>minimum = 0</b> <b>maximum = 0x7F</b> <b>step = 1</b> <b>default = 0x4D</b>	I2C Address

<u>(Below options will show at Control Logic Type set PMIC_TPS68470 or PMIC_UP6641)</u>		
WLED1 Type	[Disabled] <b>[White Led]</b> [Warm Led] [IR Led] [Xeon Led]	WLED Type
WLED1 Flash Max Current	<b>minimum = 0</b> <b>maximum = 0x1F</b> <b>step = 1</b> <b>default = 0</b>	WLED Flash Max Current Valid range is 0x00-0x1F 0x00 for HW default max current
WLED1 Torch Max Current	<b>minimum = 0</b> <b>maximum = 0x7</b> <b>step = 1</b> <b>default = 0</b>	WLED Torch Max Current Valid range is 0x00-0x07 0x00 for HW default max current
WLED2 Type	[Disabled] [White Led] [Warm Led] <b>[IR Led]</b> [Xeon Led]	WLED Type
WLED2 Flash Max Current	<b>minimum = 0</b> <b>maximum = 0x1F</b> <b>step = 1</b> <b>default = 0</b>	WLED Flash Max Current Valid range is 0x00-0x1F 0x00 for HW default max current
WLED2 Torch Max Current	<b>minimum = 0</b> <b>maximum = 0x7</b> <b>step = 1</b> <b>default = 0</b>	WLED Torch Max Current Valid range is 0x00-0x07 0x00 for HW default max current
SubPlatformId	<b>minimum = 0</b> <b>maximum = 0xF</b> <b>step = 1</b> <b>default = 0</b>	SubPlatformId
<u>(Below options will show at Control Logic Type set Discrete or PMIC_TPS68470 or PMIC_UP6641)</u>		
Number of GPIO Pins	<b>minimum = 0</b> <b>maximum = 4</b> <b>step = 1</b> <b>default = 0</b>	Number of GPIO Pins
<u>(Below options will show at Number of GPIO Pins set 1 or 2 or 3 or 4)</u>		
GPIO 0		
Group Pad Number	<b>minimum = 0</b> <b>maximum = 23</b> <b>step = 1</b> <b>default = 22</b>	Group Pad Number
Group Number	[A] [B] [C] <b>[D]</b> [E] [F] [G] [H]	Group Number
Function	<b>[Reset]</b> [Power_En] [Clock_En] [pLED_En]	Function
Active Value	<b>minimum = 0</b> <b>maximum = 1</b> <b>step = 1</b> <b>default = 1</b>	Active Value

Initial Value	<b>minimum = 0</b> <b>maximum = 1</b> <b>step = 1</b> <b>default = 0</b>	Initial Value
<u>(Below options will show at Number of GPIO Pins set 2 or 3 or 4)</u>		
GPIO 1		
Group Pad Number	<b>minimum = 0</b> <b>maximum = 23</b> <b>step = 1</b> <b>default = 11</b>	Group Pad Number
Group Number	[A] [B] [C] [ <b>D</b> ] [E] [F] [G] [H]	Group Number
Function	<b>[Reset]</b> [Power_En] [Clock_En] [pLED_En]	Function
Active Value	<b>minimum = 0</b> <b>maximum = 1</b> <b>step = 1</b> <b>default = 1</b>	Active Value
Initial Value	<b>minimum = 0</b> <b>maximum = 1</b> <b>step = 1</b> <b>default = 0</b>	Initial Value
<u>(Below options will show at Number of GPIO Pins set 3 or 4)</u>		
GPIO 2		
Group Pad Number	<b>minimum = 0</b> <b>maximum = 23</b> <b>step = 1</b> <b>default = 11</b>	Group Pad Number
Group Number	[A] [B] [C] [ <b>D</b> ] [E] [F] [G] [H]	Group Number
Function	<b>[Reset]</b> [Power_En] [Clock_En] [pLED_En]	Function
Active Value	<b>minimum = 0</b> <b>maximum = 1</b> <b>step = 1</b> <b>default = 1</b>	Active Value
Initial Value	<b>minimum = 0</b> <b>maximum = 1</b> <b>step = 1</b> <b>default = 0</b>	Initial Value
<u>(Below options will show at Number of GPIO Pins set 4)</u>		
GPIO 3		
Group Pad Number	<b>minimum = 0</b> <b>maximum = 23</b>	Group Pad Number

	<b>step = 1</b> <b>default = 11</b>	
Group Number	[A] [B] [C] [ <b>D</b> ] [E] [F] [G] [H]	Group Number
Function	[ <b>Reset</b> ] [Power_En] [Clock_En] [pLED_En]	Function
Active Value	<b>minimum = 0</b> <b>maximum = 1</b> <b>step = 1</b> <b>default = 1</b>	Active Value
Initial Value	<b>minimum = 0</b> <b>maximum = 1</b> <b>step = 1</b> <b>default = 0</b>	Initial Value

### 2.2.15..8.4 Control Logic options

**Table 2-2-15-8-4. Control Logic options**

BIOS Setting	Options	Description
Control Logic options		
Control Logic Type	[Discrete] [ <b>PMIC_TPS68470</b> ] [PMIC_UP6641] [PMIC_USER0] [PMIC_USER1]	Control Logic Type
CRD Version	[PTC] [CRD-D] [CRD-G] [Kilshon-PPV] [ <b>CRD-G2</b> ]	CRD Version
Input Clock	[ <b>20 MHz</b> ] [24 MHz] [26 MHz] [19.2 MHz]	Input Clock
PCH Clock Source	[ <b>IMGCLKOUT_0</b> ] [IMGCLKOUT_1]	This option specifies which IMGCLKOUT is chosen (This option will show at Control Logic Type set Discrete or Control Logic Type set PMIC_TPS68470 and CRD Version set CRD-G3)
PMIC Flash Panel	[Front] [ <b>Back</b> ]	PMIC Flash Panel (This option will show at CRD Version set CRD-G or CRD-G2)
<u>(Below options will show at Control Logic Type set PMIC_TPS68470 or PMIC_UP6641 or PMIC_USER0 or PMIC_USER1)</u>		
I2C Channel	[I2C0] [I2C1] [ <b>I2C2</b> ] [I2C3] [I2C4] [I2C5]	I2C Channel
I2C Address	<b>minimum = 0</b> <b>maximum = 0x7F</b> <b>step = 1</b> <b>default = 0x4D</b>	I2C Address

<u>(Below options will show at Control Logic Type set PMIC_TPS68470 or PMIC_UP6641)</u>		
WLED1 Type	[Disabled] [ <b>White Led</b> ] [Warm Led] [IR Led] [Xeon Led]	WLED Type
WLED1 Flash Max Current	<b>minimum = 0</b> <b>maximum = 0x1F</b> <b>step = 1</b> <b>default = 0</b>	WLED Flash Max Current Valid range is 0x00-0x1F 0x00 for HW default max current
WLED1 Torch Max Current	<b>minimum = 0</b> <b>maximum = 0x7</b> <b>step = 1</b> <b>default = 0</b>	WLED Torch Max Current Valid range is 0x00-0x07 0x00 for HW default max current
WLED2 Type	[Disabled] [White Led] [Warm Led] [ <b>IR Led</b> ] [Xeon Led]	WLED Type
WLED2 Flash Max Current	<b>minimum = 0</b> <b>maximum = 0x1F</b> <b>step = 1</b> <b>default = 0</b>	WLED Flash Max Current Valid range is 0x00-0x1F 0x00 for HW default max current
WLED2 Torch Max Current	<b>minimum = 0</b> <b>maximum = 0x7</b> <b>step = 1</b> <b>default = 0</b>	WLED Torch Max Current Valid range is 0x00-0x07 0x00 for HW default max current
SubPlatformId	<b>minimum = 0</b> <b>maximum = 0xF</b> <b>step = 1</b> <b>default = 0</b>	SubPlatformId
<u>(Below options will show at Control Logic Type set Discrete or PMIC_TPS68470 or PMIC_UP6641)</u>		
Number of GPIO Pins	<b>minimum = 0</b> <b>maximum = 4</b> <b>step = 1</b> <b>default = 0</b>	Number of GPIO Pins
<u>(Below options will show at Number of GPIO Pins set 1 or 2 or 3 or 4)</u>		
GPIO 0		
Group Pad Number	<b>minimum = 0</b> <b>maximum = 23</b> <b>step = 1</b> <b>default = 22</b>	Group Pad Number
Group Number	[A] [B] [C] [ <b>D</b> ] [E] [F] [G] [H]	Group Number
Function	[ <b>Reset</b> ] [Power_En] [Clock_En] [pLED_En]	Function
Active Value	<b>minimum = 0</b> <b>maximum = 1</b> <b>step = 1</b> <b>default = 1</b>	Active Value

Initial Value	<b>minimum = 0</b> <b>maximum = 1</b> <b>step = 1</b> <b>default = 0</b>	Initial Value
<u>(Below options will show at Number of GPIO Pins set 2 or 3 or 4)</u>		
GPIO 1		
Group Pad Number	<b>minimum = 0</b> <b>maximum = 23</b> <b>step = 1</b> <b>default = 11</b>	Group Pad Number
Group Number	[A] [B] [C] [ <b>D</b> ] [E] [F] [G] [H]	Group Number
Function	<b>[Reset]</b> [Power_En] [Clock_En] [pLED_En]	Function
Active Value	<b>minimum = 0</b> <b>maximum = 1</b> <b>step = 1</b> <b>default = 1</b>	Active Value
Initial Value	<b>minimum = 0</b> <b>maximum = 1</b> <b>step = 1</b> <b>default = 0</b>	Initial Value
<u>(Below options will show at Number of GPIO Pins set 3 or 4)</u>		
GPIO 2		
Group Pad Number	<b>minimum = 0</b> <b>maximum = 23</b> <b>step = 1</b> <b>default = 11</b>	Group Pad Number
Group Number	[A] [B] [C] [ <b>D</b> ] [E] [F] [G] [H]	Group Number
Function	<b>[Reset]</b> [Power_En] [Clock_En] [pLED_En]	Function
Active Value	<b>minimum = 0</b> <b>maximum = 1</b> <b>step = 1</b> <b>default = 1</b>	Active Value
Initial Value	<b>minimum = 0</b> <b>maximum = 1</b> <b>step = 1</b> <b>default = 0</b>	Initial Value
<u>(Below options will show at Number of GPIO Pins set 4)</u>		
GPIO 3		
Group Pad Number	<b>minimum = 0</b> <b>maximum = 23</b>	Group Pad Number

	<b>step = 1</b> <b>default = 11</b>	
Group Number	[A] [B] [C] [ <b>D</b> ] [E] [F] [G] [H]	Group Number
Function	<b>[Reset]</b> [Power_En] [Clock_En] [pLED_En]	Function
Active Value	<b>minimum = 0</b> <b>maximum = 1</b> <b>step = 1</b> <b>default = 1</b>	Active Value
Initial Value	<b>minimum = 0</b> <b>maximum = 1</b> <b>step = 1</b> <b>default = 0</b>	Initial Value

### 2.2.15.8.5 Link options

**Table 2-2-15-8-5. Link options**

BIOS Setting	Options	Description
Camera1		
Sensor Model	<b>[OV16860]</b> [OV8856] [OV9234] [IMX135] [OV5693] [IMX179] [OV8858] [OV2740- IVCAM] [OV9728] [IMX188] [IMX208] [OV5670] [OV8865] [HM2051] [OV2742] [User Custom]	Sensor Model
Custom HID	<b>minsize = 6</b> <b>maxsize = 8</b>	Custom HID (This option will show at Sensor Model set User Custom)
Lanes Clock division	<b>[4 4 2 2]</b> [4 4 3 1] [4 4 4 0] [8 0 2 2] [8 0 3 1] [8 0 4 0]	Lanes Clock division
CRD Version	[PTC] [CRD-D] [CRD-G] [Kilshon- PPV] <b>[CRD-G2]</b>	CRD Version
GPIO control	[No Control Logic] <b>[Control Logic 1]</b> [Control Logic 2] [Control Logic 3] [Control Logic 4]	GPIO control (Option [Control Logic #] will show at Control Logic # Enabled)
Camera position	[Front] <b>[Back]</b>	Camera position
Flash Support	[Driver default] [Disabled] <b>[Enabled]</b>	Flash Support
Privacy LED	<b>[Driver default]</b> [ILED A, 16mA] [ILED B, 2mA] [ILED B, 4mA]	Privacy LED

	[ILEDDB, 8mA] [ILEDDB, 16mA]	
Rotation	<b>[0]</b> [90] [180] [270]	Rotation
PMIC Position	<b>[Position 1]</b> [Position 2]	PMIC Position Position 1 indicates the current module is placed on the left side of the CRD-G2 card Position 2 indicates the current module is placed on the right side of the CRD-G2 card Position 3 indicates the current sensor is placed at the shared power rail position; it is only used on CRD-G3 card.
Voltage Rail	<b>[3 voltage rail]</b> [2 voltage rail]	Voltage Rail (This option will show at PMIC Position set Position 2)
Camera module name	<b>minsize = 1</b> <b>maxsize = 15</b> <b>default = "A16V04E"</b>	Camera module name
LaneUsed	[x1] [x2] [x3] <b>[x4]</b> [x8]	LaneUsed
MCLK	<b>minimum = 6000000</b> <b>maximum = 27000000</b> <b>step = 100000</b> <b>default = 19200000</b>	MCLK
EEPROM Type	[ROM_NONE] [ROM_OTP] [ROM_EEPROM_16K_64] [ROM_EEPROM_16K_16] [ROM_OTP_ACPI_ACPI] [ROM_ACPI] [ROM_EEPROM_BRCA016GWZ] [ROM_EEPROM_24AA32] [ROM_EEPROM_CAT24C08] <b>[ROM_EEPROM_M24C64]</b> [ROM_EEPROM_DW9806B]	EEPROM Type
VCM Type	[VCM_NONE] [VCM_AD5823] [VCM_DW9714] [VCM_AD5816] [VCM_DW9719] [VCM_DW9718] [VCM_DW9806B] [VCM_WV517S] [VCM_LC898122XA] <b>[VCM_LC898212AXB]</b> [VCM_RESERVED1] [VCM_RESERVED2]	VCM Type
Number of I2C Components	<b>minimum = 0</b> <b>maximum = 12</b>	Number of I2C Components

	<b>step = 1</b> <b>default = 1</b>	
I2C Channel	[I2C0] [I2C1] [ <b>I2C2</b> ] [I2C3] [I2C4] [I2C5]	I2C Channel
<u>(Below options will show at Number of I2C Components &gt; 0)</u>		
Device 0		
I2C Address	<b>minimum = 0</b> <b>maximum = 0x7F</b> <b>step = 1</b> <b>default = 0x10</b>	I2C Address
Device Type	<b>[Sensor]</b> [VCM] [EEPROM] [EEPROM_EXT1] [EEPROM_EXT2] [EEPROM_EXT3] [EEPROM_EXT4] [EEPROM_EXT5] [EEPROM_EXT6] [EEPROM_EXT7] [IO Expander] [Flash]	Device Type
<u>(Below options will show at Number of I2C Components &gt; 1)</u>		
Device 1		
I2C Address	<b>minimum = 0</b> <b>maximum = 0x7F</b> <b>step = 1</b> <b>default = 0x72</b>	I2C Address
Device Type	[Sensor] <b>[VCM]</b> [EEPROM] [EEPROM_EXT1] [EEPROM_EXT2] [EEPROM_EXT3] [EEPROM_EXT4] [EEPROM_EXT5] [EEPROM_EXT6] [EEPROM_EXT7] [IO Expander] [Flash]	Device Type
<u>(Below options will show at Number of I2C Components &gt; 2)</u>		
Device 2		
I2C Address	<b>minimum = 0</b> <b>maximum = 0x7F</b> <b>step = 1</b> <b>default = 0x51</b>	I2C Address
Device Type	[Sensor] [VCM] <b>[EEPROM]</b> [EEPROM_EXT1] [EEPROM_EXT2] [EEPROM_EXT3] [EEPROM_EXT4]	Device Type

	[EEPROM_EXT5] [EEPROM_EXT6] [EEPROM_EXT7] [IO Expander] [Flash]	
<u>(Below options will show at Number of I2C Components &gt; 3)</u>		
Device 3		
I2C Address	<b>minimum = 0</b> <b>maximum = 0x7F</b> <b>step = 1</b> <b>default = 0x51</b>	I2C Address
Device Type	[Sensor] [VCM] [EEPROM] <b>[EEPROM_EXT1]</b> [EEPROM_EXT2] [EEPROM_EXT3] [EEPROM_EXT4] [EEPROM_EXT5] [EEPROM_EXT6] [EEPROM_EXT7] [IO Expander] [Flash]	Device Type
<u>(Below options will show at Number of I2C Components &gt; 4)</u>		
Device 4		
I2C Address	<b>minimum = 0</b> <b>maximum = 0x7F</b> <b>step = 1</b> <b>default = 0x52</b>	I2C Address
Device Type	[Sensor] [VCM] [EEPROM] [EEPROM_EXT1][ <b>EEPROM_EXT2</b> ] [EEPROM_EXT3] [EEPROM_EXT4] [EEPROM_EXT5] [EEPROM_EXT6] [EEPROM_EXT7] [IO Expander] [Flash]	Device Type
<u>(Below options will show at Number of I2C Components &gt; 5)</u>		
Device 5		
I2C Address	<b>minimum = 0</b> <b>maximum = 0x7F</b> <b>step = 1</b> <b>default = 0x53</b>	I2C Address
Device Type	[Sensor] [VCM] [EEPROM] [EEPROM_EXT1][EEPROM_EXT2] <b>[EEPROM_EXT3]</b>	Device Type

	[EEPROM_EXT4] [EEPROM_EXT5] [EEPROM_EXT6] [EEPROM_EXT7] [IO Expander] [Flash]	
<u>(Below options will show at Number of I2C Components &gt; 6)</u>		
Device 6		
I2C Address	<b>minimum = 0</b> <b>maximum = 0x7F</b> <b>step = 1</b> <b>default = 0x54</b>	I2C Address
Device Type	[Sensor] [VCM] [EEPROM] [EEPROM_EXT1] [EEPROM_EXT2] [EEPROM_EXT3] <b>[EEPROM_EXT4]</b> [EEPROM_EXT5] [EEPROM_EXT6] [EEPROM_EXT7] [IO Expander] [Flash]	Device Type
<u>(Below options will show at Number of I2C Components &gt; 7)</u>		
Device 7		
I2C Address	<b>minimum = 0</b> <b>maximum = 0x7F</b> <b>step = 1</b> <b>default = 0x55</b>	I2C Address
Device Type	[Sensor] [VCM] [EEPROM] [EEPROM_EXT1] [EEPROM_EXT2] [EEPROM_EXT3] [EEPROM_EXT4] <b>[EEPROM_EXT5]</b> [EEPROM_EXT6] [EEPROM_EXT7] [IO Expander] [Flash]	Device Type
<u>(Below options will show at Number of I2C Components &gt; 8)</u>		
Device 8		
I2C Address	<b>minimum = 0</b> <b>maximum = 0x7F</b> <b>step = 1</b> <b>default = 0x56</b>	I2C Address
Device Type	[Sensor] [VCM] [EEPROM] [EEPROM_EXT1][EEPROM_EXT2] [EEPROM_EXT3] [EEPROM_EXT4] [EEPROM_EXT5]	Device Type

	<b>[EEPROM_EXT6]</b> [EEPROM_EXT7] [IO Expander] [Flash]	
<u>(Below options will show at Number of I2C Components &gt; 9)</u>		
Device 9		
I2C Address	<b>minimum = 0</b> <b>maximum = 0x7F</b> <b>step = 1</b> <b>default = 0x57</b>	I2C Address
Device Type	[Sensor] [VCM] [EEPROM] [EEPROM_EXT1][EEPROM_EXT2] [EEPROM_EXT3] [EEPROM_EXT4] [EEPROM_EXT5] [EEPROM_EXT6] <b>[EEPROM_EXT7]</b> [IO Expander] [Flash]	Device Type
<u>(Below options will show at Number of I2C Components &gt; 10)</u>		
Device 10		
I2C Address	<b>minimum = 0</b> <b>maximum = 0x7F</b> <b>step = 1</b> <b>default = 0x58</b>	I2C Address
Device Type	[Sensor] [VCM] [EEPROM] [EEPROM_EXT1] [EEPROM_EXT2] [EEPROM_EXT3] [EEPROM_EXT4] [EEPROM_EXT5] [EEPROM_EXT6] [EEPROM_EXT7] <b>[IO Expander]</b> [Flash]	Device Type
<u>(Below options will show at Number of I2C Components &gt; 11)</u>		
Device 11		
I2C Address	<b>minimum = 0</b> <b>maximum = 0x7F</b> <b>step = 1</b> <b>default = 0x59</b>	I2C Address
Device Type	[Sensor] [VCM] [EEPROM] [EEPROM_EXT1][EEPROM_EXT2] [EEPROM_EXT3] [EEPROM_EXT4]	Device Type

	[EEPROM_EXT5] [EEPROM_EXT6] [EEPROM_EXT7] [IO Expander] <b>[Flash]</b>	
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### 2.2.15.8.6 Link options

**Table 2-2-15-8-6. Link options**

BIOS Setting	Options	Description
Camera2		
Sensor Model	[OV16860] [OV8856] <b>[OV9234]</b> [IMX135] [OV5693] [IMX179] [OV8858] [OV2740- IVCAM] [OV9728] [IMX188] [IMX208] [OV5670] [OV8865] [HM2051] [OV2742] [User Custom]	Sensor Model
Custom HID	<b>minsize = 6</b> <b>maxsize = 8</b>	Custom HID (This option will show at Sensor Model set User Custom)
Lanes Clock division	<b>[4 4 2 2]</b> [4 4 3 1] [4 4 4 0] [8 0 2 2] [8 0 3 1] [8 0 4 0]	Lanes Clock division
CRD Version	[PTC] [CRD-D] [CRD-G] [Kilshon- PPV] <b>[CRD-G2]</b>	CRD Version
GPIO control	[No Control Logic] <b>[Control Logic 1]</b> [Control Logic 2] [Control Logic 3] [Control Logic 4]	GPIO control (Option [Control Logic #] will show at Control Logic # Enabled)
Camera position	<b>[Front]</b> [Back]	Camera position
Flash Support	[Driver default] [Disabled] <b>[Enabled]</b>	Flash Support
Privacy LED	<b>[Driver default]</b> [ILED A, 16mA] [ILED B, 2mA] [ILED B, 4mA] [ILED B, 8mA] [ILED B, 16mA]	Privacy LED
Rotation	<b>[0]</b> [90] [180] [270]	Rotation
PMIC Position	[Position 1] <b>[Position 2]</b>	PMIC Position Position 1 indicates the current module is placed on the left side of the CRD-G2 card Position 2 indicates the current module is placed on the right side of the CRD-G2 card

		Position 3 indicates the current sensor is placed at the shared power rail position; it is only used on CRD-G3 card.
Voltage Rail	<b>[3 voltage rail]</b> [2 voltage rail]	Voltage Rail (This option will show at PMIC Position set Position 2)
Camera module name	<b>minsize = 1</b> <b>maxsize = 15</b> <b>default = "6BF115T2"</b>	Camera module name
LaneUsed	<b>[x1]</b> [x2] [x3] [x4]	LaneUsed
MCLK	<b>minimum = 6000000</b> <b>maximum = 27000000</b> <b>step = 100000</b> <b>default = 19200000</b>	MCLK
EEPROM Type	<b>[ROM_NONE]</b> [ROM_OTP] [ROM_EEPROM_16K_64] [ROM_EEPROM_16K_16] [ROM_OTP_ACPI_ACPI] [ROM_ACPI] [ROM_EEPROM_BRCA016GWZ] [ROM_EEPROM_24AA32] [ROM_EEPROM_CAT24C08] [ROM_EEPROM_M24C64] [ROM_EEPROM_DW9806B]	EEPROM Type
VCM Type	<b>[VCM_NONE]</b> [VCM_AD5823] [VCM_DW9714] [VCM_AD5816] [VCM_DW9719] [VCM_DW9718] [VCM_DW9806B] [VCM_WV517S] [VCM_LC898122XA] [VCM_LC898212AXB] [VCM_RESERVED1] [VCM_RESERVED2]	VCM Type
Number of I2C Components	<b>minimum = 0</b> <b>maximum = 12</b> <b>step = 1</b> <b>default = 1</b>	Number of I2C Components
I2C Channel	[I2C0] [I2C1] <b>[I2C2]</b> [I2C3] [I2C4] [I2C5]	I2C Channel
(Below options will show at Number of I2C Components > 0)		
Device 0		
I2C Address	<b>minimum = 0</b> <b>maximum = 0x7F</b> <b>step = 1</b>	I2C Address

	<b>default = 0x36</b>	
Device Type	<b>[Sensor]</b> [VCM] [EEPROM] [EEPROM_EXT1] [EEPROM_EXT2] [EEPROM_EXT3] [EEPROM_EXT4] [EEPROM_EXT5] [EEPROM_EXT6] [EEPROM_EXT7] [IO Expander] [Flash]	Device Type
<u>(Below options will show at Number of I2C Components &gt; 1)</u>		
Device 1		
I2C Address	<b>minimum = 0</b> <b>maximum = 0x7F</b> <b>step = 1</b> <b>default = 0x0C</b>	I2C Address
Device Type	[Sensor] <b>[VCM]</b> [EEPROM] [EEPROM_EXT1] [EEPROM_EXT2] [EEPROM_EXT3] [EEPROM_EXT4] [EEPROM_EXT5] [EEPROM_EXT6] [EEPROM_EXT7] [IO Expander] [Flash]	Device Type
<u>(Below options will show at Number of I2C Components &gt; 2)</u>		
Device 2		
I2C Address	<b>minimum = 0</b> <b>maximum = 0x7F</b> <b>step = 1</b> <b>default = 0x50</b>	I2C Address
Device Type	[Sensor] [VCM] <b>[EEPROM]</b> [EEPROM_EXT1] [EEPROM_EXT2] [EEPROM_EXT3] [EEPROM_EXT4] [EEPROM_EXT5] [EEPROM_EXT6] [EEPROM_EXT7] [IO Expander] [Flash]	Device Type
<u>(Below options will show at Number of I2C Components &gt; 3)</u>		
Device 3		
I2C Address	<b>minimum = 0</b> <b>maximum = 0x7F</b> <b>step = 1</b>	I2C Address

	<b>default = 0x51</b>	
Device Type	[Sensor] [VCM] [EEPROM] <b>[EEPROM_EXT1]</b> [EEPROM_EXT2] [EEPROM_EXT3] [EEPROM_EXT4] [EEPROM_EXT5] [EEPROM_EXT6] [EEPROM_EXT7] [IO Expander] [Flash]	Device Type
<u>(Below options will show at Number of I2C Components &gt; 4)</u>		
Device 4		
I2C Address	<b>minimum = 0</b> <b>maximum = 0x7F</b> <b>step = 1</b> <b>default = 0x52</b>	I2C Address
Device Type	[Sensor] [VCM] [EEPROM] [EEPROM_EXT1][ <b>EEPROM_EXT2</b> ] [EEPROM_EXT3] [EEPROM_EXT4] [EEPROM_EXT5] [EEPROM_EXT6] [EEPROM_EXT7] [IO Expander] [Flash]	Device Type
<u>(Below options will show at Number of I2C Components &gt; 5)</u>		
Device 5		
I2C Address	<b>minimum = 0</b> <b>maximum = 0x7F</b> <b>step = 1</b> <b>default = 0x53</b>	I2C Address
Device Type	[Sensor] [VCM] [EEPROM] [EEPROM_EXT1][EEPROM_EXT2] <b>[EEPROM_EXT3]</b> [EEPROM_EXT4] [EEPROM_EXT5] [EEPROM_EXT6] [EEPROM_EXT7] [IO Expander] [Flash]	Device Type
<u>(Below options will show at Number of I2C Components &gt; 6)</u>		
Device 6		
I2C Address	<b>minimum = 0</b> <b>maximum = 0x7F</b> <b>step = 1</b>	I2C Address

	<b>default = 0x54</b>	
Device Type	[Sensor] [VCM] [EEPROM] [EEPROM_EXT1] [EEPROM_EXT2] [EEPROM_EXT3] <b>[EEPROM_EXT4]</b> [EEPROM_EXT5] [EEPROM_EXT6] [EEPROM_EXT7] [IO Expander] [Flash]	Device Type
<u>(Below options will show at Number of I2C Components &gt; 7)</u>		
Device 7		
I2C Address	<b>minimum = 0</b> <b>maximum = 0x7F</b> <b>step = 1</b> <b>default = 0x55</b>	I2C Address
Device Type	[Sensor] [VCM] [EEPROM] [EEPROM_EXT1] [EEPROM_EXT2] [EEPROM_EXT3] [EEPROM_EXT4] <b>[EEPROM_EXT5]</b> [EEPROM_EXT6] [EEPROM_EXT7] [IO Expander] [Flash]	Device Type
<u>(Below options will show at Number of I2C Components &gt; 8)</u>		
Device 8		
I2C Address	<b>minimum = 0</b> <b>maximum = 0x7F</b> <b>step = 1</b> <b>default = 0x56</b>	I2C Address
Device Type	[Sensor] [VCM] [EEPROM] [EEPROM_EXT1][EEPROM_EXT2] [EEPROM_EXT3] [EEPROM_EXT4] [EEPROM_EXT5] <b>[EEPROM_EXT6]</b> [EEPROM_EXT7] [IO Expander] [Flash]	Device Type
<u>(Below options will show at Number of I2C Components &gt; 9)</u>		
Device 9		
I2C Address	<b>minimum = 0</b> <b>maximum = 0x7F</b>	I2C Address

	<b>step = 1</b> <b>default = 0x57</b>	
Device Type	[Sensor] [VCM] [EEPROM] [EEPROM_EXT1][EEPROM_EXT2] [EEPROM_EXT3] [EEPROM_EXT4] [EEPROM_EXT5] [EEPROM_EXT6] <b>[EEPROM_EXT7]</b> [IO Expander] [Flash]	Device Type
<u>(Below options will show at Number of I2C Components &gt; 10)</u>		
Device 10		
I2C Address	<b>minimum = 0</b> <b>maximum = 0x7F</b> <b>step = 1</b> <b>default = 0x58</b>	I2C Address
Device Type	[Sensor] [VCM] [EEPROM] [EEPROM_EXT1] [EEPROM_EXT2] [EEPROM_EXT3] [EEPROM_EXT4] [EEPROM_EXT5] [EEPROM_EXT6] [EEPROM_EXT7] <b>[IO Expander]</b> [Flash]	Device Type
<u>(Below options will show at Number of I2C Components &gt; 11)</u>		
Device 11		
I2C Address	<b>minimum = 0</b> <b>maximum = 0x7F</b> <b>step = 1</b> <b>default = 0x59</b>	I2C Address
Device Type	[Sensor] [VCM] [EEPROM] [EEPROM_EXT1][EEPROM_EXT2] [EEPROM_EXT3] [EEPROM_EXT4] [EEPROM_EXT5] [EEPROM_EXT6] [EEPROM_EXT7] [IO Expander] <b>[Flash]</b>	Device Type

### 2.2.15.8.7 Link options

**Table 2-2-15-8-7. Link options**

BIOS Setting	Options	Description
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Camera3		
Sensor Model	[OV16860] <b>[OV8856]</b> [OV9234] [IMX135] [OV5693] [IMX179] [OV8858] [OV2740- IVCAM] [OV9728] [IMX188] [IMX208] [OV5670] [OV8865] [HM2051] [OV2742] [User Custom]	Sensor Model
Custom HID	<b>minsize = 6</b> <b>maxsize = 8</b>	Custom HID (This option will show at Sensor Model set User Custom)
Lanes Clock division	<b>[4 4 2 2]</b> [4 4 3 1] [4 4 4 0] [8 0 2 2] [8 0 3 1] [8 0 4 0]	Lanes Clock division
CRD Version	[PTC] <b>[CRD-D]</b> [CRD-G] [Kilshon- PPV] [CRD-G2]	CRD Version
GPIO control	[No Control Logic] [Control Logic 1] <b>[Control Logic 2]</b> [Control Logic 3] [Control Logic 4]	GPIO control (Option [Control Logic #] will show at Control Logic # Enabled)
Camera position	<b>[Front]</b> [Back]	Camera position
Flash Support	[Driver default] <b>[Disabled]</b> [Enabled]	Flash Support
Privacy LED	<b>[Driver default]</b> [ILED A, 16mA] [ILED B, 2mA] [ILED B, 4mA] [ILED B, 8mA] [ILED B, 16mA]	Privacy LED
Rotation	<b>[0]</b> [90] [180] [270]	Rotation
PMIC Position	<b>[Position 1]</b> [Position 2]	PMIC Position Position 1 indicates the current module is placed on the left side of the CRD-G2 card Position 2 indicates the current module is placed on the right side of the CRD-G2 card Position 3 indicates the current sensor is placed at the shared power rail position; it is only used on CRD-G3 card.
Voltage Rail	<b>[3 voltage rail]</b> [2 voltage rail]	Voltage Rail (This option will show at PMIC Position set Position 2)
Camera module name	<b>minsize = 1</b> <b>maxsize = 15</b>	Camera module name

	<b>default = "D8V10L"</b>	
LaneUsed	[x1] [x2] [x3] <b>[x4]</b>	LaneUsed
MCLK	<b>minimum = 6000000</b> <b>maximum = 27000000</b> <b>step = 100000</b> <b>default = 19200000</b>	MCLK
EEPROM Type	[ROM_NONE] <b>[ROM_OTP]</b> [ROM_EEPROM_16K_64] [ROM_EEPROM_16K_16] [ROM_OTP_ACPI_ACPI] [ROM_ACPI] [ROM_EEPROM_BRCA016GWZ] [ROM_EEPROM_24AA32] [ROM_EEPROM_CAT24C08] [ROM_EEPROM_M24C64] [ROM_EEPROM_DW9806B]	EEPROM Type
VCM Type	<b>[VCM_NONE]</b> [VCM_AD5823] [VCM_DW9714] [VCM_AD5816] [VCM_DW9719] [VCM_DW9718] [VCM_DW9806B] [VCM_WV517S] [VCM_LC898122XA] [VCM_LC898212AXB] [VCM_RESERVED1] [VCM_RESERVED2]	VCM Type
Number of I2C Components	<b>minimum = 0</b> <b>maximum = 12</b> <b>step = 1</b> <b>default = 1</b>	Number of I2C Components
I2C Channel	[I2C0] [I2C1] [I2C2] <b>[I2C3]</b> [I2C4] [I2C5]	I2C Channel
<u>(Below options will show at Number of I2C Components &gt; 0)</u>		
Device 0		
I2C Address	<b>minimum = 0</b> <b>maximum = 0x7F</b> <b>step = 1</b> <b>default = 0x10</b>	I2C Address
Device Type	<b>[Sensor]</b> [VCM] [EEPROM] [EEPROM_EXT1] [EEPROM_EXT2] [EEPROM_EXT3] [EEPROM_EXT4] [EEPROM_EXT5] [EEPROM_EXT6] [EEPROM_EXT7] [IO Expander]	Device Type

	[Flash]	
<u>(Below options will show at Number of I2C Components &gt; 1)</u>		
Device 1		
I2C Address	<b>minimum = 0</b> <b>maximum = 0x7F</b> <b>step = 1</b> <b>default = 0x0E</b>	I2C Address
Device Type	[Sensor] <b>[VCM]</b> [EEPROM] [EEPROM_EXT1] [EEPROM_EXT2] [EEPROM_EXT3] [EEPROM_EXT4] [EEPROM_EXT5] [EEPROM_EXT6] [EEPROM_EXT7] [IO Expander] [Flash]	Device Type
<u>(Below options will show at Number of I2C Components &gt; 2)</u>		
Device 2		
I2C Address	<b>minimum = 0</b> <b>maximum = 0x7F</b> <b>step = 1</b> <b>default = 0x50</b>	I2C Address
Device Type	[Sensor] [VCM] <b>[EEPROM]</b> [EEPROM_EXT1] [EEPROM_EXT2] [EEPROM_EXT3] [EEPROM_EXT4] [EEPROM_EXT5] [EEPROM_EXT6] [EEPROM_EXT7] [IO Expander] [Flash]	Device Type
<u>(Below options will show at Number of I2C Components &gt; 3)</u>		
Device 3		
I2C Address	<b>minimum = 0</b> <b>maximum = 0x7F</b> <b>step = 1</b> <b>default = 0x51</b>	I2C Address
Device Type	[Sensor] [VCM] [EEPROM] <b>[EEPROM_EXT1]</b> [EEPROM_EXT2] [EEPROM_EXT3] [EEPROM_EXT4] [EEPROM_EXT5] [EEPROM_EXT6] [EEPROM_EXT7] [IO Expander]	Device Type

	[Flash]	
<u>(Below options will show at Number of I2C Components &gt; 4)</u>		
Device 4		
I2C Address	<b>minimum = 0</b> <b>maximum = 0x7F</b> <b>step = 1</b> <b>default = 0x52</b>	I2C Address
Device Type	[Sensor] [VCM] [EEPROM] [EEPROM_EXT1][ <b>EEPROM_EXT2</b> ] [EEPROM_EXT3] [EEPROM_EXT4] [EEPROM_EXT5] [EEPROM_EXT6] [EEPROM_EXT7] [IO Expander] [Flash]	Device Type
<u>(Below options will show at Number of I2C Components &gt; 5)</u>		
Device 5		
I2C Address	<b>minimum = 0</b> <b>maximum = 0x7F</b> <b>step = 1</b> <b>default = 0x53</b>	I2C Address
Device Type	[Sensor] [VCM] [EEPROM] [EEPROM_EXT1][EEPROM_EXT2] <b>[EEPROM_EXT3]</b> [EEPROM_EXT4] [EEPROM_EXT5] [EEPROM_EXT6] [EEPROM_EXT7] [IO Expander] [Flash]	Device Type
<u>(Below options will show at Number of I2C Components &gt; 6)</u>		
Device 6		
I2C Address	<b>minimum = 0</b> <b>maximum = 0x7F</b> <b>step = 1</b> <b>default = 0x54</b>	I2C Address
Device Type	[Sensor] [VCM] [EEPROM] [EEPROM_EXT1] [EEPROM_EXT2] [EEPROM_EXT3] <b>[EEPROM_EXT4]</b> [EEPROM_EXT5] [EEPROM_EXT6] [EEPROM_EXT7] [IO Expander]	Device Type

	[Flash]	
<u>(Below options will show at Number of I2C Components &gt; 7)</u>		
Device 7		
I2C Address	<b>minimum = 0</b> <b>maximum = 0x7F</b> <b>step = 1</b> <b>default = 0x55</b>	I2C Address
Device Type	[Sensor] [VCM] [EEPROM] [EEPROM_EXT1] [EEPROM_EXT2] [EEPROM_EXT3] [EEPROM_EXT4] <b>[EEPROM_EXT5]</b> [EEPROM_EXT6] [EEPROM_EXT7] [IO Expander] [Flash]	Device Type
<u>(Below options will show at Number of I2C Components &gt; 8)</u>		
Device 8		
I2C Address	<b>minimum = 0</b> <b>maximum = 0x7F</b> <b>step = 1</b> <b>default = 0x56</b>	I2C Address
Device Type	<b>[Sensor]</b> [VCM] [EEPROM] [EEPROM_EXT1][EEPROM_EXT2] [EEPROM_EXT3] [EEPROM_EXT4] [EEPROM_EXT5] [EEPROM_EXT6] [EEPROM_EXT7] [IO Expander] [Flash]	Device Type
<u>(Below options will show at Number of I2C Components &gt; 9)</u>		
Device 9		
I2C Address	<b>minimum = 0</b> <b>maximum = 0x7F</b> <b>step = 1</b> <b>default = 0x57</b>	I2C Address
Device Type	<b>[Sensor]</b> [VCM] [EEPROM] [EEPROM_EXT1][EEPROM_EXT2] [EEPROM_EXT3] [EEPROM_EXT4] [EEPROM_EXT5] [EEPROM_EXT6] [EEPROM_EXT7] [IO Expander]	Device Type

	[Flash]	
<u>(Below options will show at Number of I2C Components &gt; 10)</u>		
Device 10		
I2C Address	<b>minimum = 0</b> <b>maximum = 0x7F</b> <b>step = 1</b> <b>default = 0x58</b>	I2C Address
Device Type	<b>[Sensor]</b> [VCM] [EEPROM] [EEPROM_EXT1][EEPROM_EXT2] [EEPROM_EXT3] [EEPROM_EXT4] [EEPROM_EXT5] [EEPROM_EXT6] [EEPROM_EXT7] [IO Expander] [Flash]	Device Type
<u>(Below options will show at Number of I2C Components &gt; 11)</u>		
Device 11		
I2C Address	<b>minimum = 0</b> <b>maximum = 0x7F</b> <b>step = 1</b> <b>default = 0x59</b>	I2C Address
Device Type	<b>[Sensor]</b> [VCM] [EEPROM] [EEPROM_EXT1][EEPROM_EXT2] [EEPROM_EXT3] [EEPROM_EXT4] [EEPROM_EXT5] [EEPROM_EXT6] [EEPROM_EXT7] [IO Expander] [Flash]	Device Type

### 2.2.15.8.8 Link options

**Table 2-2-15-8-8. Link options**

BIOS Setting	Options	Description
Camera4		
Sensor Model	[OV16860] [OV8856] <b>[OV9234]</b> [IMX135] [OV5693] [IMX179] [OV8858] [OV2740- IVCAM] [OV9728] [IMX188] [IMX208] [OV5670] [OV8865] [HM2051] [OV2742] [User Custom]	Sensor Model
Custom HID	<b>minsize = 6</b>	Custom HID

	<b>maxsize = 8</b>	(This option will show at Sensor Model set User Custom)
Lanes Clock division	<b>[4 4 2 2]</b> [4 4 3 1] [4 4 4 0] [8 0 2 2] [8 0 3 1] [8 0 4 0]	Lanes Clock division
CRD Version	[PTC] [CRD-D] [CRD-G] [Kilshon-PPV] <b>[CRD-G2]</b>	CRD Version
GPIO control	[No Control Logic] <b>[Control Logic 1]</b> [Control Logic 2] [Control Logic 3] [Control Logic 4]	GPIO control (Option [Control Logic #] will show at Control Logic # Enabled)
Camera position	<b>[Front]</b> [Back]	Camera position
Flash Support	[Driver default] [Disabled] <b>[Enabled]</b>	Flash Support
Privacy LED	<b>[Driver default]</b> [ILEDA, 16mA] [ILEDB, 2mA] [ILEDB, 4mA] [ILEDB, 8mA] [ILEDB, 16mA]	Privacy LED
Rotation	<b>[0]</b> [90] [180] [270]	Rotation
PMIC Position	[Position 1] <b>[Position 2]</b>	PMIC Position Position 1 indicates the current module is placed on the left side of the CRD-G2 card Position 2 indicates the current module is placed on the right side of the CRD-G2 card Position 3 indicates the current sensor is placed at the shared power rail position; it is only used on CRD-G3 card.
Voltage Rail	<b>[3 voltage rail]</b> [2 voltage rail]	Voltage Rail (This option will show at PMIC Position set Position 2)
Camera module name	<b>minsize = 1</b> <b>maxsize = 15</b> <b>default = "6BF115T2"</b>	Camera module name
LaneUsed	<b>[x1]</b> [x2] [x3] [x4]	LaneUsed
MCLK	<b>minimum = 6000000</b> <b>maximum = 27000000</b> <b>step = 100000</b> <b>default = 19200000</b>	MCLK

EEPROM Type	<b>[ROM_NONE]</b> [ROM_OTP] [ROM_EEPROM_16K_64] [ROM_EEPROM_16K_16] [ROM_OTP_ACPI_ACPI] [ROM_ACPI] [ROM_EEPROM_BRCA016GWZ] [ROM_EEPROM_24AA32] [ROM_EEPROM_CAT24C08] [ROM_EEPROM_M24C64] [ROM_EEPROM_DW9806B]	EEPROM Type
VCM Type	<b>[VCM_NONE]</b> [VCM_AD5823] [VCM_DW9714] [VCM_AD5816] [VCM_DW9719] [VCM_DW9718] [VCM_DW9806B] [VCM_WV517S] [VCM_LC898122XA] [VCM_LC898212AXB] [VCM_RESERVED1] [VCM_RESERVED2]	VCM Type
Number of I2C Components	<b>minimum = 0</b> <b>maximum = 12</b> <b>step = 1</b> <b>default = 1</b>	Number of I2C Components
I2C Channel	[I2C0] [I2C1] <b>[I2C2]</b> [I2C3] [I2C4] [I2C5]	I2C Channel
<u>(Below options will show at Number of I2C Components &gt; 0)</u>		
Device 0		
I2C Address	<b>minimum = 0</b> <b>maximum = 0x7F</b> <b>step = 1</b> <b>default = 0x36</b>	I2C Address
Device Type	<b>[Sensor]</b> [VCM] [EEPROM] [EEPROM_EXT1] [EEPROM_EXT2] [EEPROM_EXT3] [EEPROM_EXT4] [EEPROM_EXT5] [EEPROM_EXT6] [EEPROM_EXT7] [IO Expander] [Flash]	Device Type
<u>(Below options will show at Number of I2C Components &gt; 1)</u>		
Device 1		
I2C Address	<b>minimum = 0</b> <b>maximum = 0x7F</b> <b>step = 1</b> <b>default = 0x0C</b>	I2C Address

Device Type	[Sensor] <b>[VCM]</b> [EEPROM] [EEPROM_EXT1] [EEPROM_EXT2] [EEPROM_EXT3] [EEPROM_EXT4] [EEPROM_EXT5] [EEPROM_EXT6] [EEPROM_EXT7] [IO Expander] [Flash]	Device Type
<u>(Below options will show at Number of I2C Components &gt; 2)</u>		
Device 2		
I2C Address	<b>minimum = 0</b> <b>maximum = 0x7F</b> <b>step = 1</b> <b>default = 0x50</b>	I2C Address
Device Type	[Sensor] [VCM] <b>[EEPROM]</b> [EEPROM_EXT1] [EEPROM_EXT2] [EEPROM_EXT3] [EEPROM_EXT4] [EEPROM_EXT5] [EEPROM_EXT6] [EEPROM_EXT7] [IO Expander] [Flash]	Device Type
<u>(Below options will show at Number of I2C Components &gt; 3)</u>		
Device 3		
I2C Address	<b>minimum = 0</b> <b>maximum = 0x7F</b> <b>step = 1</b> <b>default = 0x51</b>	I2C Address
Device Type	[Sensor] [VCM] [EEPROM] <b>[EEPROM_EXT1]</b> [EEPROM_EXT2] [EEPROM_EXT3] [EEPROM_EXT4] [EEPROM_EXT5] [EEPROM_EXT6] [EEPROM_EXT7] [IO Expander] [Flash]	Device Type
<u>(Below options will show at Number of I2C Components &gt; 4)</u>		
Device 4		
I2C Address	<b>minimum = 0</b> <b>maximum = 0x7F</b> <b>step = 1</b> <b>default = 0x52</b>	I2C Address

Device Type	[Sensor] [VCM] [EEPROM] [EEPROM_EXT1][ <b>EEPROM_EXT2</b> ] [EEPROM_EXT3] [EEPROM_EXT4] [EEPROM_EXT5] [EEPROM_EXT6] [EEPROM_EXT7] [IO Expander] [Flash]	Device Type
<u>(Below options will show at Number of I2C Components &gt; 5)</u>		
Device 5		
I2C Address	<b>minimum = 0</b> <b>maximum = 0x7F</b> <b>step = 1</b> <b>default = 0x53</b>	I2C Address
Device Type	[Sensor] [VCM] [EEPROM] [EEPROM_EXT1][EEPROM_EXT2] <b>[EEPROM_EXT3]</b> [EEPROM_EXT4] [EEPROM_EXT5] [EEPROM_EXT6] [EEPROM_EXT7] [IO Expander] [Flash]	Device Type
<u>(Below options will show at Number of I2C Components &gt; 6)</u>		
Device 6		
I2C Address	<b>minimum = 0</b> <b>maximum = 0x7F</b> <b>step = 1</b> <b>default = 0x54</b>	I2C Address
Device Type	[Sensor] [VCM] [EEPROM] [EEPROM_EXT1] [EEPROM_EXT2] [EEPROM_EXT3] <b>[EEPROM_EXT4]</b> [EEPROM_EXT5] [EEPROM_EXT6] [EEPROM_EXT7] [IO Expander] [Flash]	Device Type
<u>(Below options will show at Number of I2C Components &gt; 7)</u>		
Device 7		
I2C Address	<b>minimum = 0</b> <b>maximum = 0x7F</b> <b>step = 1</b> <b>default = 0x55</b>	I2C Address

Device Type	[Sensor] [VCM] [EEPROM] [EEPROM_EXT1] [EEPROM_EXT2] [EEPROM_EXT3] [EEPROM_EXT4] <b>[EEPROM_EXT5]</b> [EEPROM_EXT6] [EEPROM_EXT7] [IO Expander] [Flash]	Device Type
<u>(Below options will show at Number of I2C Components &gt; 8)</u>		
Device 8		
I2C Address	<b>minimum = 0</b> <b>maximum = 0x7F</b> <b>step = 1</b> <b>default = 0x56</b>	I2C Address
Device Type	[Sensor] [VCM] [EEPROM] [EEPROM_EXT1][EEPROM_EXT2] [EEPROM_EXT3] [EEPROM_EXT4] [EEPROM_EXT5] <b>[EEPROM_EXT6]</b> [EEPROM_EXT7] [IO Expander] [Flash]	Device Type
<u>(Below options will show at Number of I2C Components &gt; 9)</u>		
Device 9		
I2C Address	<b>minimum = 0</b> <b>maximum = 0x7F</b> <b>step = 1</b> <b>default = 0x57</b>	I2C Address
Device Type	[Sensor] [VCM] [EEPROM] [EEPROM_EXT1][EEPROM_EXT2] [EEPROM_EXT3] [EEPROM_EXT4] [EEPROM_EXT5] [EEPROM_EXT6] <b>[EEPROM_EXT7]</b> [IO Expander] [Flash]	Device Type
<u>(Below options will show at Number of I2C Components &gt; 10)</u>		
Device 10		
I2C Address	<b>minimum = 0</b> <b>maximum = 0x7F</b> <b>step = 1</b> <b>default = 0x58</b>	I2C Address

Device Type	[Sensor] [VCM] [EEPROM] [EEPROM_EXT1][EEPROM_EXT2] [EEPROM_EXT3] [EEPROM_EXT4] [EEPROM_EXT5] [EEPROM_EXT6] [EEPROM_EXT7] <b>[IO Expander]</b> [Flash]	Device Type
<u>(Below options will show at Number of I2C Components &gt; 11)</u>		
Device 11		
I2C Address	<b>minimum = 0</b> <b>maximum = 0x7F</b> <b>step = 1</b> <b>default = 0x59</b>	I2C Address
Device Type	[Sensor] [VCM] [EEPROM] [EEPROM_EXT1][EEPROM_EXT2] [EEPROM_EXT3] [EEPROM_EXT4] [EEPROM_EXT5] [EEPROM_EXT6] [EEPROM_EXT7] [IO Expander] <b>[Flash]</b>	Device Type

## 2.2.16 PCIE Configuration

**Table 2-2-16. PCIE Configuration**

BIOS Setting	Options	Description
PCIE Configuration		
IMR Configuration	(See Section 2.2.16.1)	IMR Configuration

### 2.2.16.1 IMR Configuration

**Table 2-2-16-1. IMR Configuration**

BIOS Setting	Options	Description
IMR Configuration		
PCIe IMR	<b>[Disable]</b> [Enable]	Enable/Disable PCIe IMR <i>(Below will show at this option set Enable)</i>
PCIe IMR Size	<b>minimum = 0</b> <b>maximum = 1024</b> <b>step = 1</b> <b>default = 0</b>	PCIe Reserved Memory Size to be requested in MB. Maximum value of 1024 MB

PCIe RP Location for IMR	<b>[PCH PCIE]</b> [SA PCIE]	Select SA or PCH root port associated with IMR
RP index for IMR	<b>minimum = 0</b> <b>maximum = 3</b> <b>step = 1</b> <b>default = 0</b>	Selects which root port will be associated with IMR

## 2.2.17 PCH-IO Configuration

**Table 2-2-17. PCH-IO Configuration**

BIOS Setting	Options	Description
PCH-IO Configuration		
PCI Express Configuration	(See Section 2.2.17.1)	PCI Express Configuration settings
SATA Configuration	(See Section 2.2.17.2)	SATA Device Options Settings
USB Configuration	(See Section 2.2.17.3)	USB Configuration settings
Security Configuration	(See Section 2.2.17.4)	Security Configuration settings
HD Audio Configuration	(See Section 2.2.17.5)	HD Audio Subsystem Configuration Settings (Show as <u>SETUP_VOLATILE_DATA.PlatformFlavor</u> is not FlavorUpServer)
THC Configuration	(See Section 2.2.17.6)	Touch Host Controller Configuration Settings
Serial IO Configuration	(See Section 2.2.17.7)	Serial IO Configuration Settings
SCS Configuration	(See Section 2.2.17.8)	Storage and Communication Subsystem (SCS) Configuration
ISH Configuration	(See Section 2.2.17.9)	Integrated Sensor Hub (ISH) Configuration
Pch Thermal Throttling Control	(See Section 2.2.17.10)	Pch Thermal Throttling Control
Skip VCC In Configuration	<b>[Disable]</b> [Enable]	Skips VCC In Configuration if enabled
FIVR Configuration	(See Section 2.2.17.11)	Menu for changing FIVR configuration parameters
PMC Configuration	(See Section 2.2.17.12)	Power management controller configuration
(Show as <u>SETUP_VOLATILE_DATA.GbeSupportByPch</u> is not 0)		
PCH LAN Controller	<b>[Enabled]</b> [Disabled]	Enable/Disable onboard NIC. (Show as <u>SETUP_VOLATILE_DATA.GbeAvailable</u> is not 0)

(Below options will show at PCH LAN Controller set Enabled and GbeAvailable)		
LAN Wake From DeepSx	<b>[Enabled]</b> [Disabled]	Wake from DeepSx by the assertion of LAN_WAKE# pin
Wake on LAN Enable	<b>[Enabled]</b> [Disabled]	Enable/Disable integrated LAN to wake the system.
SLP_LAN# Low on DC Power	<b>[Enabled]</b> [Disabled]	Enable/Disable SLP_LAN# Low on DC Power.
Foxville I225 LAN Controller	<b>[Enabled]</b> [Disabled]	Enable/Disable Foxville I225 LAN Controller.
Foxville I225 Wake on LAN Support	<b>[Enabled]</b> [Disabled]	Enable/Disable Foxville I225 Wake on LAN Support.
EFI Network	[Onboard NIC] [WiFi] [Onboard NIC & WiFi] <b>[Disabled]</b>	Enable/Disable EFI Network support for onboard LAN or WiFi module. <u>([Onboard NIC] &amp; [Onboard NIC &amp; WiFi] options will show at PCH LAN Controller set Enabled and GbeAvailable)</u>
Sensor Hub Type	[None] <b>[I2C Sensor Hub]</b> [USB Sensor Hub]	Choose the Sensor Hub Type, 'None' will Suppress 'I2C Sensor Hub' Setup Option, 'I2C' Will Suppress 'ALS' Setup Option and 'USB' will Suppress Both I2C and ALS. (Show as <u>SETUP_VOLATILE_DATA.PlatformFlavor</u> is not FlavorMobile AND <u>SETUP_VOLATILE_DATA.PlatformFlavor</u> is not FlavorEmbedded)
DeepSx Power Policies	<b>[Disabled]</b> [Enabled in S4-S5/Battery] [Enabled in S4-S5]	configure the DeepSx Mode configuration.
PS_ON Enable	[Enabled] <b>[Disabled]</b>	Enable or disable PS_ON ()support a new C10 state from the CPU on desktop SKUs that enables a lower power target that will be required by the California Energy Commission (CEC). (Show as <u>SETUP_VOLATILE_DATA.PlatformFlavor</u> is not FlavorDesktop)
Wake on WLAN and BT Enable	[Enabled] <b>[Disabled]</b>	Enable/Disable PCI Express Wireless LAN and Bluetooth to wake the system. <u>(Below option will show at this option set Enabled)</u>
DeepSx Wake on WLAN and BT Enable	[Enabled] <b>[Disabled]</b>	Enable/Disable PCI Express Wireless LAN and Bluetooth to wake the system from DeepSx.
Disable DSX ACPRESENT PullDown	[Enabled] <b>[Disabled]</b>	Disable PCH internal ACPRESENT PullDown when DeepSx or G3 exit.

State After G3	<b>[S0 State]</b> [S5 State]	Specify what state to go to when power is re-applied after a power failure (G3 state).
Port 80h Redirection	<b>[LPC Bus]</b> [PCIE Bus]	Control where the Port 80h cycles are sent. (Below option can be set at this option set LPC Bus)
Enhance Port 80h LPC Decoding	[Disabled] <b>[Enabled]</b>	Support the word/dword decoding of port 80h behind LPC
Compatible Revision ID	<b>[Disabled]</b> [Enabled]	Enable/Disable the PCH Compatible Revision ID feature (Show as <u>SETUP_VOLATILE_DATA.PchCridSupport</u> is not 0)
Legacy IO Low Latency	<b>[Disabled]</b> [Enabled]	Set to enable low latency of legacy IO. Some systems require lower IO latency irrespective of power. This is a tradeoff between power and IO latency.
PCH Cross Throttling	[Disabled] <b>[Enabled]</b>	Enable/Disable the PCH Cross Throttling feature. Only ULT support this feature.
PCH Energy Reporting	[Disabled] <b>[Enabled]</b>	Enable Energy Report. MUST set it as ENABLED. This is only for test purpose.
LPM S0i2.0	[Disabled] <b>[Enabled]</b>	Enable/Disable S0ix sub-state. This setting is for test purpose. S0ix sub-states should be enabled for production.
LPM S0i3.0	[Disabled] <b>[Enabled]</b>	Enable/Disable S0ix sub-state. This setting is for test purpose. S0ix sub-states should be enabled for production.
C10 Dynamic threshold adjustment	<b>[Disabled]</b> [Enabled]	Enable/Disable C10 dynamic threshold adjustment
IEH Mode	<b>[Bypass Mode]</b> [Enabled]	Enable/Bypass IEH Mode
Enable TCO Timer	SIMICS_FLAG is defined: [Disabled] [Enabled]  else: <b>[Disabled]</b> [Enabled]	Enable/Disable TCO timer. When disabled, it disables PCH ACPI timer, stops TCO timer, and ACPI WDAT table will not be published.
Pcie Pll SSC	<b>[Auto]</b> [0.0%] [0.1%] [0.2%] [0.3%] [0.4%] [0.5%] [0.6%] [0.7%] [0.8%] [0.9%] [1.0%] [1.1%] [1.2%] [1.3%] [1.4%] [1.5%] [1.6%] [1.7%] [1.8%] [1.9%] [2.0%]	Pcie Pll SSC percentage. AUTO - Keep hw default, no BIOS override. Range is 0.0%-2.0%.
IOAPIC 24-119 Entries	[Disabled] <b>[Enabled]</b>	Enables/Disables IOAPIC 24-119 Entries. IRQ24-119 may be used by

		PCH devices. Disabling those interrupts may cause certain devices failure. (Show as <u>SETUP_VOLATILE_DATA.PlatformType</u> is not TypeUltUlx AND <u>SETUP_VOLATILE_DATA.PlatformFlavor</u> is not FlavorUpServer)
Enable 8254 Clock Gate	[Disabled] <b>[Enabled]</b> [Enabled In Runtime and S3 Resume]	Enables/Disables 8254 clock gate in early phase. Set 8254CGE is necessary for SLP_S0 support. Platform is able to disable this policy and set 8254CGE in late phase. (This option will show at tLow Power S0 Idle Capability set Enabled)
Lock PCH Sideband Access	[Disabled] <b>[Enabled]</b>	Lock PCH Sideband access, include SideBand interface lock and SideBand PortID mask for certain end point (e.g. PSFx). The option is invalid if POSTBOOT SAI is set.
Flash Protection Range Registers (FPRR)	[Disabled] <b>[Enabled]</b>	Enable Flash Protection Range Registers
SPD Write Disable	<b>[True]</b> [False]	Enable/Disable setting SPD Write Disable. For security recommendations, SPD write disable bit must be set.
LGMR	[Enabled] <b>[Disabled]</b>	64KB memory block for LGMR (LPC Memory Range Decode)
HOST_C10 reporting to Target	[Enabled] <b>[Disabled]</b>	This option enables HOST_C10 reporting to Target via eSPI Virtual Wire
OS IDLE Mode	[Disabled] <b>[Enabled]</b>	Enable/Disable OS Idle Mode Feature
S0ix Auto Demotion	[Disabled] <b>[Enabled]</b>	Enable/Disable Host Low Power Mode S0ix Auto-Demotion
Latch Events C10 Exit	[Enabled] <b>[Disabled]</b>	Enable/Disable Latch Events on C10 Exit
Hybrid Storage Detection and Configuration Mode	[Dynamic Configuration for Hybrid Storage Enable] <b>[Disabled]</b>	Select Hybrid Storage Detection and Configuration Mode (Below will show at this option not Disabled)
Cpu Root port used for hybrid storag	<b>minimum = 0</b> <b>maximum = 0xFF</b> <b>step = 1</b> <b>default = 0xFF</b>	Select cpu root port used for hybrid storage value between 0 to 2
Extended BIOS Range Decode	[Enabled] <b>[Disabled]</b>	Enabling this will make memory cycles falling in a specific area to be redirected to SPI flash controller
ACPI L6D PME Handling	[Enabled] <b>[Disabled]</b>	BIOS through ACPI code can associate specific method to a particular GPE. In this case _L6D for Level-triggered

		Event, BIOS-ACPI can verify PMEENABLE and PMESTATUS of each device that requires GPE related wake.
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### 2.2.17.1 PCI Express Configuration

**Table 2-2-17-1. PCI Express Configuration**

BIOS Setting	Options	Description
PCI Express Configuration		
PCI Express Clock Gating	[Disabled] <b>[Enabled]</b>	PCI Express Clock Gating Enable/Disable for each root port.
DMI Link ASPM Control	[Disabled] [L0s] [L1] [L0sL1] <b>[Auto]</b>	The control of Active State Power Management of the DMI Link.
Port8xh Decode	<b>[Disabled]</b> [Enabled]	PCI Express Port8xh Decode Enable/Disable.
Port8xh Decode Port#	<b>minimum = 0</b> <b>maximum = 23</b> <b>step = 1</b> <b>default = 0</b>	Select PCI Express Port8xh Decode Root Port. User to ensure port availability
Peer Memory Write Enable	<b>[Disabled]</b> [Enabled]	Peer Memory Write Enable/Disable
Compliance Test Mode	<b>[Disabled]</b> [Enabled]	Enable when using Compliance Load Board
PCIe function swap	[Disabled] <b>[Enabled]</b>	When Disabled, prevents PCIe rootport function swap. If any function other than 0th is enabled, 0th will become visible.
PCIe EQ settings	(See Section 2.2.17.1.1)	This form contains options for controlling PCIe EQ process
IMR Configuration	(See Section 2.2.17.1.2)	IMR Configuration
PCI Express Root Port #	PciePortCfg[PORT_INDEX] == PCH_RP_AVAILABLE; (See Section 2.2.17.1.3)	PCI Express Root Port Settings. PciePortCfg[PORT_INDEX] == PCH_RP_FUSED_OFF Not present in this SKU PCH_RP_MERGED Shadowed by x2/x4 port PCH_RP_DIFFERENT_BUS Lane configured as USB/SATA/UFS PCH_RP_ETHERNET Reserved for ethernet PCH_RP_NOT_IMPLEMENTED Display nothing
PCIe clocks	(See Section 2.2.17.1.4)	PCIe clocks

### 2.2.17.1.1 PCIe EQ settings

**Table 2-2-17-1-1. PCIe EQ settings**

BIOS Setting	Options	Description
PCIe EQ settings		
PCIe EQ override	<b>[Disabled]</b> [Enable]	Choose your own PCIe EQ settings, only for users who have a thorough understanding of equalization process <i>(Below will show at this option set Enable)</i>
PCIe EQ method	<b>[PCIe hardware EQ]</b> [PCIe fixed EQ]	Choose PCIe EQ method
PCIe EQ mode	<b>[Use presets during EQ]</b> [Use coefficients during EQ]	Choose EQ mode. Preset mode - root port will use presets during EQ process, Coefficient mode - root port will use coefficients during EQ process
EQ PH1 downstream port transmitter preset	<b>minimum = 0</b> <b>maximum = 10</b> <b>step = 1</b> <b>default = 0</b>	Choose the value of the preset that will be used during phase 1 of the equalization
EQ PH1 upstream port transmitter preset"	<b>minimum = 0</b> <b>maximum = 10</b> <b>step = 1</b> <b>default = 0</b>	Choose the value of the preset that will be used during phase 1 of the equalization
Enable EQ phase 2 local transmitter override	<b>[Disabled]</b> [Enable]	EQ Phase 2 local transmitter override can be used to debug issues with PCI devices equalization.
EQ Phase 2 local transmitter override preset	<b>minimum = 0</b> <b>maximum = 10</b> <b>step = 1</b> <b>default = 0</b>	Select preset which will be used during phase 2 of the PCIe EQ process <i>(This will show at Enable EQ phase 2 local transmitter override set to Enable)</i>
Number of presets or coefficients used during phase 3	<b>minimum = 0</b> <b>maximum = 11</b> <b>step = 1</b> <b>default = 0</b>	Select how many presets or coefficients will be used during phase 3 of EQ. Please not that you have to set all of the list entries to valid values. The interpretation of this field depends on PCIe EQ mode
Perset # {# is number from 0 to 10}	<b>minimum = 0</b> <b>maximum = 63</b> <b>step = 1</b> <b>default = 0</b>	Choose the target preset value <i>(This option will show at PCIe EQ method set to PCIe EQ method)</i>

Pre-cursor coefficient # {# is number from 0 to 9}	<b>minimum = 0</b> <b>maximum = 63</b> <b>step = 1</b> <b>default = 0</b>	Choose the target pre-cursor coefficient value <i>(This option will show at PCIe EQ method set to PCIe fixed EQ)</i>
Post-cursor coefficient # {# is number from 0 to 9}	<b>minimum = 0</b> <b>maximum = 63</b> <b>step = 1</b> <b>default = 0</b>	Choose the target post-cursor coefficient value <i>(This option will show at PCIe EQ method set to PCIe fixed EQ)</i>

### 2.2.17.1.2 IMR Configuration

**Table 2-2-17-1-2. IMR Configuration**

BIOS Setting	Options	Description
PCIe IMR	<b>[Disabled]</b> [Enabled]	Enable/Disable PCIe IMR <i>(Below options will show at this option set Enabled)</i>
PCIe IMR Size	<b>minimum = 0</b> <b>maximum = 1024</b> <b>step = 1</b> <b>default = 0</b>	PCIe Reserved Memory Size to be requested in MB. Maximum value of 1024 MB
RP index for IMR	<b>minimum = 1</b> <b>maximum = 24</b> <b>step = 1</b> <b>default = 1</b>	Selects which root port will be associated with IMR

### 2.2.17.1.3 PCI Express Root Port #

**Table 2-2-17-1-3. PCI Express Root Port #**

BIOS Setting	Options	Description
PCI Express Root Port #	[Disabled] <b>[Enabled]</b>	Control the PCI Express Root Port.
Disable Gen2 Pll Shutdown and L1 Controller Power gating	<b>[Disabled]</b> [Enabled]	When Enabled, disables Gen2 PLL Shutdown and L1 Controller power gating, Enable this option if using Titan Ridge A0/Alpine Ridge thunderbolt controller
<i>(Below options will show at PCI Express Root Port # set Enabled)</i>		
Topology	<b>[Board specific]</b> [Unknown] [x1] [x4] [Sata Express] [M2]	Identify the SATA Topology if it is Default or ISATA or Flex or DirectConnect or M2
Connection Type	[Built-in] <b>[Slot]</b>	Built-In: a built-in device is connected to this rootport. SlotImplemented bit will be clear. Slot: this rootport connects to

		user-accessible slot. SlotImplemented bit will be set. (This option can be set at Hot Plug set Disabled)
ASPM	[Disabled] [L0s] [L1] [L0sL1] <b>[Auto]</b>	PCI Express Active State Power Management settings.
L1 Substates	[Disabled] [L1.1] <b>[L1.1 &amp; L1.2]</b>	PCI Express L1 Substates settings.
Gen3 Eq Phase3 Method	<b>[Hardware]</b> [Static Coeff.]	PCIe Gen3 Equalization Phase 3 Method
UPTP	<b>minimum = 0</b> <b>maximum = 10</b> <b>step = 1</b> <b>default = 5</b>	Upstream Port Transmitter Preset
DPTP	<b>minimum = 0</b> <b>maximum = 10</b> <b>step = 1</b> <b>default = 7</b>	Downstream Port Transmitter Preset
ACS	[Disabled] <b>[Enabled]</b>	Enable/Disable Access Control Services Extended Capability
PTM	[Disabled] <b>[Enabled]</b>	Enable/Disable Precision Time Measurement
DPC	[Disabled] <b>[Enabled]</b>	Enable/Disable Downstream Port Containment
EDPC	[Disabled] <b>[Enabled]</b>	Enable/Disable Rootport extensions for Downstream Port Containment
URR	<b>[Disabled]</b> [Enabled]	PCI Express Unsupported Request Reporting Enable/Disable.
FER	<b>[Disabled]</b> [Enabled]	PCI Express Device Fatal Error Reporting Enable/Disable.
NFER	<b>[Disabled]</b> [Enabled]	PCI Express Device Non-Fatal Error Reporting Enable/Disable.
CER	<b>[Disabled]</b> [Enabled]	PCI Express Device Correctable Error Reporting Enable/Disable.
CTO	<b>[Disabled]</b> [Enabled]	PCI Express Completion Timer TO Enable/Disable.
SEFE	<b>[Disabled]</b> [Enabled]	Root PCI Express System Error on Fatal Error Enable/Disable.
SENF	<b>[Disabled]</b> [Enabled]	Root PCI Express System Error on Non-Fatal Error Enable/Disable.
SECE	<b>[Disabled]</b> [Enabled]	Root PCI Express System Error on Correctable Error Enable/Disable.
PME SCI	[Disabled] <b>[Enabled]</b>	PCI Express PME SCI Enable/Disable.

Hot Plug	<b>[Disabled]</b> [Enabled]	PCI Express Hot Plug Enable/Disable. (This option can be set at Connection Type set Slot, and it will show at PCIe function swap set Enabled.)
Advanced Error Reporting	[Disabled] <b>[Enabled]</b>	Advanced Error Reporting Enable/Disable.
PCIe Speed	<b>[Auto]</b> [Gen1] [Gen2] [Gen3]	Configure PCIe Speed
Transmitter Half Swing	<b>[Disabled]</b> [Enabled]	Transmitter Half Swing Enable/Disable.
Detect Timeout	<b>minimum = 0</b> <b>maximum = 65535</b> <b>step = 1</b> <b>default = 0</b>	The number of milliseconds reference code will wait for link to exit Detect state for enabled ports before assuming there is no device and potentially disabling the port.
<u>(Below options will show at Discrete Thunderbolt(TM) Support set Disabled.)</u>		
Extra Bus Reserved	<b>minimum = 0</b> <b>maximum = 7</b> <b>step = 1</b> <b>default = 0</b>	Extra Bus Reserved (0-7) for bridges behind this Root Bridge.
Reserved Memory	<b>minimum = 1</b> <b>maximum = 20</b> <b>step = 1</b> <b>default = 10</b>	Reserved Memory for this Root Bridge (1-20) MB
Reserved I/O	<b>minimum = 4</b> <b>maximum = 20</b> <b>step = 4</b> <b>default = 4</b>	Reserved I/O (4K/8K/12K/16K/20K) Range for this Root Bridge.
PCH PCIe LTR Configuration		
LTR	[Disabled] <b>[Enabled]</b>	PCH PCIE Latency Reporting Enable/Disable (Below options will show at this options set Enabled.)
Snoop Latency Override	[Disabled] [Manual] <b>[Auto]</b>	Snoop Latency Override for PCH PCIE. Disabled: Disable override. Manual: Manually enter override values. Auto (default): Maintain default BIOS flow.
Snoop Latency Value	<b>minimum = 0</b> <b>maximum = 1023</b> <b>step = 1</b> <b>default = 60</b>	LTR Snoop Latency value of PCH PCIE

Snoop Latency Multiplier	[1 ns] [32 ns] <b>[1024 ns]</b> [32768 ns] [1048576 ns] [33554432 ns]	LTR Snoop Latency Multiplier of PCH PCIE
Non Snoop Latency Override	[Disabled] [Manual] <b>[Auto]</b>	Non Snoop Latency Override for PCH PCIE. Disabled: Disable override. Manual: Manually enter override values. Auto (default): Maintain default BIOS flow.
Non Snoop Latency Value	<b>minimum = 0</b> <b>maximum = 1023</b> <b>step = 1</b> <b>default = 60</b>	LTR Non Snoop Latency value of PCH PCIE (Below options will show at this options set Manual.)
Non Snoop Latency Multiplier	[1 ns] [32 ns] <b>[1024 ns]</b> [32768 ns] [1048576 ns] [33554432 ns]	LTR Non Snoop Latency Multiplier of PCH PCIE
Force LTR Override	<b>[Disabled]</b> [Enabled]	Force LTR Override for PCH PCIE. Disabled: LTR override values will not be forced. Enable: LTR override values will be forced and LTR messages from the device will be ignored.
LTR Lock	<b>[Disabled]</b> [Enabled]	PCIE LTR Configuration Lock

### 2.2.17.1.4 PCIE clocks

**Table 2-2-17-1-4. PCIE clocks**

BIOS Setting	Options	Description
Clock0 assignment	<b>[Platform-POR]</b> [Enabled] [Disabled]	Platform-POR = clock is assigned to PCIe port or LAN according to board layout. Enabled = keep clock enabled even if unused. Disabled = Disable clock.
ClkReq for Clock0	<b>[Platform-POR]</b> [Disabled]	Platform-POR = CLKREQ signal is assigned to CLKSRC according to board layout. Disabled = CLKREQ will not be used.
Clock1 assignment	<b>[Platform-POR]</b> [Enabled] [Disabled]	Platform-POR = clock is assigned to PCIe port or LAN according to board layout. Enabled = keep clock enabled even if unused. Disabled = Disable clock.
ClkReq for Clock1	<b>[Platform-POR]</b> [Disabled]	Platform-POR = CLKREQ signal is assigned to CLKSRC according to board layout. Disabled = CLKREQ will not be used.

Clock2 assignment	<b>[Platform-POR]</b> [Enabled] [Disabled]	Platform-POR = clock is assigned to PCIe port or LAN according to board layout. Enabled = keep clock enabled even if unused. Disabled = Disable clock.
ClkReq for Clock2	<b>[Platform-POR]</b> [Disabled]	Platform-POR = CLKREQ signal is assigned to CLKSRC according to board layout. Disabled = CLKREQ will not be used.
Clock3 assignment	<b>[Platform-POR]</b> [Enabled] [Disabled]	Platform-POR = clock is assigned to PCIe port or LAN according to board layout. Enabled = keep clock enabled even if unused. Disabled = Disable clock.
ClkReq for Clock3	<b>[Platform-POR]</b> [Disabled]	Platform-POR = CLKREQ signal is assigned to CLKSRC according to board layout. Disabled = CLKREQ will not be used.
Clock4 assignment	<b>[Platform-POR]</b> [Enabled] [Disabled]	Platform-POR = clock is assigned to PCIe port or LAN according to board layout. Enabled = keep clock enabled even if unused. Disabled = Disable clock.
ClkReq for Clock4	<b>[Platform-POR]</b> [Disabled]	Platform-POR = CLKREQ signal is assigned to CLKSRC according to board layout. Disabled = CLKREQ will not be used.
Clock5 assignment	<b>[Platform-POR]</b> [Enabled] [Disabled]	Platform-POR = clock is assigned to PCIe port or LAN according to board layout. Enabled = keep clock enabled even if unused. Disabled = Disable clock.
ClkReq for Clock5	<b>[Platform-POR]</b> [Disabled]	Platform-POR = CLKREQ signal is assigned to CLKSRC according to board layout. Disabled = CLKREQ will not be used.
Clock6 assignment	<b>[Platform-POR]</b> [Enabled] [Disabled]	Platform-POR = clock is assigned to PCIe port or LAN according to board layout. Enabled = keep clock enabled even if unused. Disabled = Disable clock.
ClkReq for Clock6	<b>[Platform-POR]</b> [Disabled]	Platform-POR = CLKREQ signal is assigned to CLKSRC according to board layout. Disabled = CLKREQ will not be used.
Clock7 assignment	<b>[Platform-POR]</b> [Enabled] [Disabled]	Platform-POR = clock is assigned to PCIe port or LAN according to board layout. Enabled = keep clock enabled even if unused. Disabled = Disable clock.

ClkReq for Clock7	<b>[Platform-POR]</b> [Disabled]	Platform-POR = CLKREQ signal is assigned to CLKSRC according to board layout. Disabled = CLKREQ will not be used.
Clock8 assignment	<b>[Platform-POR]</b> [Enabled] [Disabled]	Platform-POR = clock is assigned to PCIe port or LAN according to board layout. Enabled = keep clock enabled even if unused. Disabled = Disable clock.
ClkReq for Clock8	<b>[Platform-POR]</b> [Disabled]	Platform-POR = CLKREQ signal is assigned to CLKSRC according to board layout. Disabled = CLKREQ will not be used.
Clock9 assignment	<b>[Platform-POR]</b> [Enabled] [Disabled]	Platform-POR = clock is assigned to PCIe port or LAN according to board layout. Enabled = keep clock enabled even if unused. Disabled = Disable clock.
ClkReq for Clock9	<b>[Platform-POR]</b> [Disabled]	Platform-POR = CLKREQ signal is assigned to CLKSRC according to board layout. Disabled = CLKREQ will not be used.
Clock10 assignment	<b>[Platform-POR]</b> [Enabled] [Disabled]	Platform-POR = clock is assigned to PCIe port or LAN according to board layout. Enabled = keep clock enabled even if unused. Disabled = Disable clock.
ClkReq for Clock10	<b>[Platform-POR]</b> [Disabled]	Platform-POR = CLKREQ signal is assigned to CLKSRC according to board layout. Disabled = CLKREQ will not be used.
Clock11 assignment	<b>[Platform-POR]</b> [Enabled] [Disabled]	Platform-POR = clock is assigned to PCIe port or LAN according to board layout. Enabled = keep clock enabled even if unused. Disabled = Disable clock.
ClkReq for Clock11	<b>[Platform-POR]</b> [Disabled]	Platform-POR = CLKREQ signal is assigned to CLKSRC according to board layout. Disabled = CLKREQ will not be used.
Clock12 assignment	<b>[Platform-POR]</b> [Enabled] [Disabled]	Platform-POR = clock is assigned to PCIe port or LAN according to board layout. Enabled = keep clock enabled even if unused. Disabled = Disable clock.
ClkReq for Clock12	<b>[Platform-POR]</b> [Disabled]	Platform-POR = CLKREQ signal is assigned to CLKSRC according to board layout. Disabled = CLKREQ will not be used.

Clock13 assignment	<b>[Platform-POR]</b> [Enabled] [Disabled]	Platform-POR = clock is assigned to PCIe port or LAN according to board layout. Enabled = keep clock enabled even if unused. Disabled = Disable clock.
ClkReq for Clock13	<b>[Platform-POR]</b> [Disabled]	Platform-POR = CLKREQ signal is assigned to CLKSRC according to board layout. Disabled = CLKREQ will not be used.
Clock14 assignment	<b>[Platform-POR]</b> [Enabled] [Disabled]	Platform-POR = clock is assigned to PCIe port or LAN according to board layout. Enabled = keep clock enabled even if unused. Disabled = Disable clock.
ClkReq for Clock14	<b>[Platform-POR]</b> [Disabled]	Platform-POR = CLKREQ signal is assigned to CLKSRC according to board layout. Disabled = CLKREQ will not be used.
Clock15 assignment	<b>[Platform-POR]</b> [Enabled] [Disabled]	Platform-POR = clock is assigned to PCIe port or LAN according to board layout. Enabled = keep clock enabled even if unused. Disabled = Disable clock.
ClkReq for Clock15	<b>[Platform-POR]</b> [Disabled]	Platform-POR = CLKREQ signal is assigned to CLKSRC according to board layout. Disabled = CLKREQ will not be used.

## 2.2.17.2 SATA Configuration

**Table 2-2-17-2. SATA Configuration**

BIOS Setting	Options	Description
SATA And RST Configuration		
SATA Controller(s)	<b>[Enabled]</b> [Disabled]	Enable/Disable SATA Device. (Below options will show at this options set Enabled.)
SATA Mode Selection	<b>[AHCI]</b> [Intel RST Premium With Intel Optane System Acceleration]	Determines how SATA controller(s) operate. (Below options will show at this options set Intel RST Premium With Intel Optane System Acceleration.)
SATA Test Mode	[Enabled] <b>[Disabled]</b>	Test Mode Enable/Disable (Loop Back).
(Below options will show at SATA Test Mode set Disabled.)		
Software Feature Mask Configuration	(See Section 2.2.17.2.1)	RST Legacy OROM/RST UEFI driver will refer to the SWFM

		configuration to enable/disable the storage features
Aggressive LPM Support	[Disabled] <b>[Enabled]</b>	Enable PCH to aggressively enter link power state.
Serial ATA Port 0	No options	None
Software Preserve	No options	None
Port 0	[Disabled] <b>[Enabled]</b>	Enable or Disable SATA Port (This option will show at SATA Test Mode set Disabled.)
(Below options will show at External set Disabled.)		
Hot Plug	<b>[Disabled]</b> [Enabled]	Designates this port as Hot Pluggable.
Configured as eSATA	No options	None
External	<b>[Disabled]</b> [Enabled]	Marks this port as external.
Mechanical Presence Switch	[Disabled] <b>[Enabled]</b>	Controls reporting if this port has an Mechanical Presence Switch. Note: Requires hardware support.
Spin Up Device	<b>[Disabled]</b> [Enabled]	If enabled for any of ports Staggerred Spin Up will be performed and only the drives which have this option enabled will spin up at boot. Otherwise all drives spin up at boot.
SATA Device Type	<b>[Hard Disk Drive]</b> [Solid State Drive]	Identify the SATA port is connected to Solid State Drive or Hard Disk Drive
Topology	<b>[Unknown]</b> [ISATA] [Direct Connect] [Flex] [M2]	Identify the SATA Topology if it is Default or ISATA or Flex or DirectConnect or M2
SATA Port 0 DevSlp	<b>[Disabled]</b> [Enabled]	Enable/Disable SATA Port 0 DevSlp. For DevSlp to work, both hard drive and SATA port need to support DevSlp function, otherwise an unexpected behavior might happen. Please check board design before enabling it.
DITO Configuration	<b>[Disabled]</b> [Enabled]	Enable/Disable DITO Configuration (Below options can be set at This option set Enabled.)
DITO Value	<b>minimum = 0</b> <b>maximum = 1023</b> <b>step = 0</b> <b>default = 625</b>	DITO Value
DM Value	<b>minimum = 0</b>	DM Value

		<b>maximum = 15</b> <b>step = 0</b> <b>default = 15</b>	
Serial ATA Port 1	No options		None
Software Preserve	No options		None
Port 1	[Disabled] <b>[Enabled]</b>		Enable or Disable SATA Port (This option will show at SATA Test Mode set Disabled.)
<u>(Below options will show at External set Disabled.)</u>			
Hot Plug	<b>[Disabled]</b> [Enabled]		Designates this port as Hot Pluggable.
Configured as eSATA	No options		None
External	<b>[Disabled]</b> [Enabled]		Marks this port as external.
Mechanical Presence Switch	[Disabled] <b>[Enabled]</b>		Controls reporting if this port has an Mechanical Presence Switch. Note: Requires hardware support.
Spin Up Device	<b>[Disabled]</b> [Enabled]		If enabled for any of ports Staggered Spin Up will be performed and only the drives which have this option enabled will spin up at boot. Otherwise all drives spin up at boot.
SATA Device Type	<b>[Hard Disk Drive]</b> [Solid State Drive]		Identify the SATA port is connected to Solid State Drive or Hard Disk Drive
Topology	<b>[Unknown]</b> [ISATA] [Direct Connect] [Flex] [M2]		Identify the SATA Topology if it is Default or ISATA or Flex or DirectConnect or M2
SATA Port 1 DevSlp	<b>[Disabled]</b> [Enabled]		Enable/Disable SATA Port 1 DevSlp. For DevSlp to work, both hard drive and SATA port need to support DevSlp function, otherwise an unexpected behavior might happen. Please check board design before enabling it.
DITO Configuration	<b>[Disabled]</b> [Enabled]		Enable/Disable DITO Configuration (Below options can be set at This option set Enabled.)
DITO Value	<b>minimum = 0</b> <b>maximum = 1023</b> <b>step = 0</b> <b>default = 625</b>		DITO Value
DM Value	<b>minimum = 0</b> <b>maximum = 15</b> <b>step = 0</b>		DM Value

		<b>default = 15</b>	
Serial ATA Port 2	No options		None
Software Preserve	No options		None
Port 2	[Disabled] <b>[Enabled]</b>		Enable or Disable SATA Port (This option will show at SATA Test Mode set Disabled.)
<u>(Below options will show at External set Disabled.)</u>			
Hot Plug	<b>[Disabled]</b> [Enabled]		Designates this port as Hot Pluggable.
Configured as eSATA	No options		None
External	<b>[Disabled]</b> [Enabled]		Marks this port as external.
Mechanical Presence Switch	[Disabled] <b>[Enabled]</b>		Controls reporting if this port has an Mechanical Presence Switch. Note: Requires hardware support.
Spin Up Device	<b>[Disabled]</b> [Enabled]		If enabled for any of ports Staggered Spin Up will be performed and only the drives which have this option enabled will spin up at boot. Otherwise all drives spin up at boot.
SATA Device Type	<b>[Hard Disk Drive]</b> [Solid State Drive]		Identify the SATA port is connected to Solid State Drive or Hard Disk Drive
Topology	<b>[Unknown]</b> [ISATA] [Direct Connect] [Flex] [M2]		Identify the SATA Topology if it is Default or ISATA or Flex or DirectConnect or M2
SATA Port 2 DevSlp	<b>[Disabled]</b> [Enabled]		Enable/Disable SATA Port 2 DevSlp. For DevSlp to work, both hard drive and SATA port need to support DevSlp function, otherwise an unexpected behavior might happen. Please check board design before enabling it.
DITO Configuration	<b>[Disabled]</b> [Enabled]		Enable/Disable DITO Configuration (Below options can be set at This option set Enabled.)
DITO Value	<b>minimum = 0 maximum = 1023 step = 0 default = 625</b>		DITO Value
DM Value	<b>minimum = 0 maximum = 15 step = 0 default = 15</b>		DM Value

(Below options will show at <u>SETUP_VOLATILE_DATA.PlatformType</u> is TypeTrad.)		
Serial ATA Port 3	No options	None
Software Preserve	No options	None
Port 3	[Disabled] <b>[Enabled]</b>	Enable or Disable SATA Port (This option will show at <u>SATA Test Mode set Disabled.</u> )
<u>(Below options will show at External set Disabled.)</u>		
Hot Plug	<b>[Disabled]</b> [Enabled]	Designates this port as Hot Pluggable.
Configured as eSATA	No options	None
External	<b>[Disabled]</b> [Enabled]	Marks this port as external.
Mechanical Presence Switch	[Disabled] <b>[Enabled]</b>	Controls reporting if this port has an Mechanical Presence Switch. Note: Requires hardware support.
Spin Up Device	<b>[Disabled]</b> [Enabled]	If enabled for any of ports Staggered Spin Up will be performed and only the drives which have this option enabled will spin up at boot. Otherwise all drives spin up at boot.
SATA Device Type	<b>[Hard Disk Drive]</b> [Solid State Drive]	Identify the SATA port is connected to Solid State Drive or Hard Disk Drive
Topology	<b>[Unknown]</b> [ISATA] [Direct Connect] [Flex] [M2]	Identify the SATA Topology if it is Default or ISATA or Flex or DirectConnect or M2
SATA Port 3 DevSlp	<b>[Disabled]</b> [Enabled]	Enable/Disable SATA Port 3 DevSlp. For DevSlp to work, both hard drive and SATA port need to support DevSlp function, otherwise an unexpected behavior might happen. Please check board design before enabling it.
DITO Configuration	<b>[Disabled]</b> [Enabled]	Enable/Disable DITO Configuration (Below options can be set at <u>This option set Enabled.</u> )
DITO Value	<b>minimum = 0 maximum = 1023 step = 0 default = 625</b>	DITO Value
DM Value	<b>minimum = 0 maximum = 15 step = 0 default = 15</b>	DM Value

Serial ATA Port 4	No options	None
Software Preserve	No options	None
Port 4	[Disabled] <b>[Enabled]</b>	Enable or Disable SATA Port (This option will show at SATA Test Mode set Disabled.)
<u>(Below options will show at External set Disabled.)</u>		
Hot Plug	<b>[Disabled]</b> [Enabled]	Designates this port as Hot Pluggable.
Configured as eSATA	No options	None
External	<b>[Disabled]</b> [Enabled]	Marks this port as external.
Mechanical Presence Switch	[Disabled] <b>[Enabled]</b>	Controls reporting if this port has an Mechanical Presence Switch. Note: Requires hardware support.
Spin Up Device	<b>[Disabled]</b> [Enabled]	If enabled for any of ports Staggered Spin Up will be performed and only the drives which have this option enabled will spin up at boot. Otherwise all drives spin up at boot.
SATA Device Type	<b>[Hard Disk Drive]</b> [Solid State Drive]	Identify the SATA port is connected to Solid State Drive or Hard Disk Drive
Topology	<b>[Unknown]</b> [ISATA] [Direct Connect] [Flex] [M2]	Identify the SATA Topology if it is Default or ISATA or Flex or DirectConnect or M2
SATA Port 4 DevSlp	<b>[Disabled]</b> [Enabled]	Enable/Disable SATA Port 4 DevSlp. For DevSlp to work, both hard drive and SATA port need to support DevSlp function, otherwise an unexpected behavior might happen. Please check board design before enabling it.
DITO Configuration	<b>[Disabled]</b> [Enabled]	Enable/Disable DITO Configuration (Below options can be set at This option set Enabled.)
DITO Value	<b>minimum = 0 maximum = 1023 step = 0 default = 625</b>	DITO Value
DM Value	<b>minimum = 0 maximum = 15 step = 0 default = 15</b>	DM Value
Serial ATA Port 5	No options	None

Software Preserve	No options	None
Port 5	[Disabled] <b>[Enabled]</b>	Enable or Disable SATA Port ( <u>This option will show at SATA Test Mode set Disabled.</u> )
<u>(Below options will show at External set Disabled.)</u>		
Hot Plug	<b>[Disabled]</b> [Enabled]	Designates this port as Hot Pluggable.
Configured as eSATA	No options	None
External	<b>[Disabled]</b> [Enabled]	Marks this port as external.
Mechanical Presence Switch	[Disabled] <b>[Enabled]</b>	Controls reporting if this port has an Mechanical Presence Switch. Note: Requires hardware support.
Spin Up Device	<b>[Disabled]</b> [Enabled]	If enabled for any of ports Staggered Spin Up will be performed and only the drives which have this option enabled will spin up at boot. Otherwise all drives spin up at boot.
SATA Device Type	<b>[Hard Disk Drive]</b> [Solid State Drive]	Identify the SATA port is connected to Solid State Drive or Hard Disk Drive
Topology	<b>[Unknown]</b> [ISATA] [Direct Connect] [Flex] [M2]	Identify the SATA Topology if it is Default or ISATA or Flex or DirectConnect or M2
SATA Port 5 DevSlp	<b>[Disabled]</b> [Enabled]	Enable/Disable SATA Port 5 DevSlp. For DevSlp to work, both hard drive and SATA port need to support DevSlp function, otherwise an unexpected behavior might happen. Please check board design before enabling it.
DITO Configuration	<b>[Disabled]</b> [Enabled]	Enable/Disable DITO Configuration ( <u>Below options can be set at This option set Enabled.</u> )
DITO Value	<b>minimum = 0 maximum = 1023 step = 0 default = 625</b>	DITO Value
DM Value	<b>minimum = 0 maximum = 15 step = 0 default = 15</b>	DM Value
Serial ATA Port 6	No options	None
Software Preserve	No options	None

Port 6	[Disabled] <b>[Enabled]</b>	Enable or Disable SATA Port (This option will show at SATA Test Mode set Disabled.)
<u>(Below options will show at External set Disabled.)</u>		
Hot Plug	<b>[Disabled]</b> [Enabled]	Designates this port as Hot Pluggable.
Configured as eSATA	No options	None
External	<b>[Disabled]</b> [Enabled]	Marks this port as external.
Mechanical Presence Switch	[Disabled] <b>[Enabled]</b>	Controls reporting if this port has an Mechanical Presence Switch. Note: Requires hardware support.
Spin Up Device	<b>[Disabled]</b> [Enabled]	If enabled for any of ports Staggerred Spin Up will be performed and only the drives which have this option enabled will spin up at boot. Otherwise all drives spin up at boot.
SATA Device Type	<b>[Hard Disk Drive]</b> [Solid State Drive]	Identify the SATA port is connected to Solid State Drive or Hard Disk Drive
Topology	<b>[Unknown]</b> [ISATA] [Direct Connect] [Flex] [M2]	Identify the SATA Topology if it is Default or ISATA or Flex or DirectConnect or M2
SATA Port 6 DevSlp	<b>[Disabled]</b> [Enabled]	Enable/Disable SATA Port 6 DevSlp. For DevSlp to work, both hard drive and SATA port need to support DevSlp function, otherwise an unexpected behavior might happen. Please check board design before enabling it.
DITO Configuration	<b>[Disabled]</b> [Enabled]	Enable/Disable DITO Configuration (Below options can be set at This option set Enabled.)
DITO Value	<b>minimum = 0 maximum = 1023 step = 0 default = 625</b>	DITO Value
DM Value	<b>minimum = 0 maximum = 15 step = 0 default = 15</b>	DM Value
Serial ATA Port 7	No options	None
Software Preserve	No options	None
Port 7	[Disabled] <b>[Enabled]</b>	Enable or Disable SATA Port

		(This option will show at SATA Test Mode set Disabled.)
(Below options will show at External set Disabled.)		
Hot Plug	<b>[Disabled]</b> [Enabled]	Designates this port as Hot Pluggable.
Configured as eSATA	No options	None
External	<b>[Disabled]</b> [Enabled]	Marks this port as external.
Mechanical Presence Switch	[Disabled] <b>[Enabled]</b>	Controls reporting if this port has an Mechanical Presence Switch. Note: Requires hardware support.
Spin Up Device	<b>[Disabled]</b> [Enabled]	If enabled for any of ports Staggered Spin Up will be performed and only the drives which have this option enabled will spin up at boot. Otherwise all drives spin up at boot.
SATA Device Type	<b>[Hard Disk Drive]</b> [Solid State Drive]	Identify the SATA port is connected to Solid State Drive or Hard Disk Drive
Topology	<b>[Unknown]</b> [ISATA] [Direct Connect] [Flex] [M2]	Identify the SATA Topology if it is Default or ISATA or Flex or DirectConnect or M2
SATA Port 7 DevSlp	<b>[Disabled]</b> [Enabled]	Enable/Disable SATA Port 7 DevSlp. For DevSlp to work, both hard drive and SATA port need to support DevSlp function, otherwise an unexpected behavior might happen. Please check board design before enabling it.
DITO Configuration	<b>[Disabled]</b> [Enabled]	Enable/Disable DITO Configuration (Below options can be set at This option set Enabled.)
DITO Value	<b>minimum = 0 maximum = 1023 step = 0 default = 625</b>	DITO Value
DM Value	<b>minimum = 0 maximum = 15 step = 0 default = 15</b>	DM Value
HDD Acoustic Power Management	<b>[Disabled]</b> [Enabled]	Option to Enable or Disable HDD Acoustic Power Management
HDD Acoustic Mode	<b>[Bypass]</b> [Quiet] [Max Performance]	Option to optimize the Hard disk Performance and Acoustic Noise Level

		Bypass - Do Nothing : Compatibility Reasons Quiet - Drive is Slower, But Quieter Max Performance - Drive is Faster, but possibly Noisier
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### 2.2.17.2.1 Software Feature Mask Configuration

**Table 2-2-17-2-1 Software. Feature Mask Configuration**

BIOS Setting	Options	Description
Software Feature Mask Configuration		

### 2.2.17.3 USB Configuration

**Table 2-2-17-3. USB Configuration**

BIOS Setting	Options	Description
USB Configuration		
xDCI Support	<b>[Disabled]</b> [Enabled]	Enable/Disable xDCI (USB OTG Device).
USB2 PHY Sus Well Power Gating	[Disabled] <b>[Enabled]</b>	Select 'Enabled' to enable SUS Well PG for USB2 PHY. This option has no effect on PCH-H
USB PDO Programming	[Disabled] <b>[Enabled]</b>	Select 'Enabled' if Port Disable Override functionality is used
USB Overcurrent	[Disabled] <b>[Enabled]</b>	Select 'Disabled' for pin-based debug. If pin-based debug is enabled but USB overcurrent is not disabled, USB Dbc does not work.
USB Overcurrent Lock	[Disabled] <b>[Enabled]</b>	Select 'Enabled' if Overcurrent functionality is used. Enabling this will make xHCI controller consume the Overcurrent mapping data
USB Audio Offload	[Disabled] <b>[Enabled]</b>	Enable/Disable USB Audio Offload functionality
USB Port Disable Override	[Disabled] <b>[Select Per-Pin]</b>	Selectively Enable/Disable the corresponding USB port from reporting a Device Connection to the controller. <u>(Below options will show at this option set Select Per-Pin.)</u>
USB SS Physical Connector #0~9	[Disabled] <b>[Enabled]</b>	Enable/Disable this USB Physical Connector (physical port). Once disabled, any USB devices plug into the connector will not be detected by BIOS or OS.

		(Port6~9 will show as <u>SETUP_VOLATILE_DATA.PlatformType</u> is TypeTrad.)
USB HS Physical Connector #0~13	[Disabled] <b>[Enabled]</b>	Enable/Disable this USB Physical Connector (physical port). Once disabled, any USB devices plug into the connector will not be detected by BIOS or OS. (Port10~13 will show as <u>SETUP_VOLATILE_DATA.PlatformType</u> is TypeTrad.)
USB Sensor Hub	[Enabled] <b>[Disabled]</b>	USB Sensor Hub enable/disable (This option will show at Sensor Hub Type set USB Sensor Hub.)

### 2.2.17.4 Security Configuration

**Table 2-2-17-4. Security Configuration**

BIOS Setting	Options	Description
Security Configuration		
RTC Memory Lock	[Disabled] <b>[Enabled]</b>	Enable will lock bytes 38h-3Fh in the lower/upper 128-byte bank of RTC RAM
BIOS Lock	[Disabled] <b>[Enabled]</b>	Enable/Disable the PCH BIOS Lock Enable feature. Required to be enabled to ensure SMM protection of flash.
Force unlock on all GPIO pads	<b>[Disabled]</b> [Enabled]	If Enabled BIOS will force all GPIO pads to be in unlocked state

### 2.2.17.5 HD Audio Configuration

**Table 2-2-17-5. HD Audio Configuration**

BIOS Setting	Options	Description
HD Audio Subsystem Configuration Settings		
HD Audio	[Disabled] <b>[Enabled]</b>	Control Detection of the HD-Audio device. Disabled = HDA will be unconditionally disabled Enabled = HDA will be unconditionally enabled. (Below options will show at this option set <u>Select Enabled.</u> )
Audio DSP	[Disabled] <b>[Enabled]</b>	Enable/Disable Audio DSP.
Audio DSP Compliance Mode	<b>[Non-UAA (IntelSST)]</b> [UAA (HDA Inbox/IntelSST)]	Specifies DSP enabled system compliance:

		<p>1. Non-UAA (IntelSST driver support only – CC_040100)                  2. UAA (HD Audio Inbox or IntelSST driver support – CC_040380)</p> <p>Note: NHLT (DMIC/BT/I2S configuration) is published for non-UAA only.                  (This option will show at Audio DSP set Enabled.)</p>
HDA-Link Codec Select	<b>[Platform Onboard]</b> [External Kit]	Selects whether Platform Onboard Codec (single Verb Table installed) or External Codec Kit (multiple Verb Tables installed) will be used.
<u>(Below options will show at Audio Link Mode set Advanced Link Config.)</u>		
Advanced Link Configuration:		Muxed interfaces: 1) HDA/SSP0 2) HDA[SDI1]/SSP1 3) DMIC0/SNDW4 4) DMIC1/SNDW3\nCNL only: 5) HDA/SNDW1 6) SSP1/SNDW2
HDA Link	[Disabled] <b>[Enabled]</b>	<u>(This option can be set at SSP #0 set Disabled.)</u>
DMIC #0	[Disabled] <b>[Enabled]</b>	<u>(This option can be set at SNDW #4 set Disabled.)</u>
DMIC #1	[Disabled] <b>[Enabled]</b>	<u>(This option can be set at SNDW #3 set Disabled.)</u>
SSP #0	<b>[Disabled]</b> [Enabled]	<u>(This option can be set at HDA Link set Disabled.)</u>
SSP #1	<b>[Disabled]</b> [Enabled]	
SSP #2	<b>[Disabled]</b> [Enabled]	
SSP #3	<b>[Disabled]</b> [Enabled]	
SSP #4	<b>[Disabled]</b> [Enabled]	
SSP #5	<b>[Disabled]</b> [Enabled]	
SNDW #1	[Disabled] <b>[Enabled]</b>	
SNDW #1	<b>[Disabled]</b> [Enabled]	
SNDW #2	<b>[Disabled]</b> [Enabled]	
SNDW #3	<b>[Disabled]</b> [Enabled]	<u>(This option can be set at DMIC #0 set Disabled.)</u>

SNDW #4	<b>[Disabled]</b> [Enabled]	(This option can be set at DMIC #1 set Disabled.)
HDA-Link Codec Select	<b>[Platform Onboard]</b> [External Kit]	Selects whether Platform Onboard Codec (single Verb Table installed) or External Codec Kit (multiple Verb Tables installed) will be used.
HD Audio Advanced Configuration	(See Section 2.2.17.5.1)	HD Audio Subsystem Advanced Configuration Settings
HD Audio DSP Features Configuration	(See Section 2.2.17.5.2)	HD Audio Subsystem Features Configuration (ACPI) (This option will show at Audio DSP set Enabled.)

### 2.2.17.5.1 HD Audio Advanced Configuration

**Table 2-2-17-5-1. HD Audio Advanced Configuration**

BIOS Setting	Options	Description
HD Audio Subsystem Advanced Configuration Settings		
iDisplay Audio Disconnect	<b>[Disabled]</b> [Enabled]	Disconnects SDI2 signal to hide/disable iDisplay Audio Codec.
Codec Sx Wake Capability	<b>[Disabled]</b> [Enabled]	Capability to detect wake initiated by a codec in Sx (eg by modem codec)
PME Enable	<b>[Disabled]</b> [Enabled]	Enables PME wake of HD Audio controller during POST.
Statically Switchable BCLK Clock Frequency Configuration:		Statically Switchable BCLK Clock Frequency Configuration:
HD Audio Link Frequency	[6 MHz] [12 MHz] <b>[24 MHz]</b>	Selects HD Audio Link frequency. Applicable only if HDA codec supports selected frequency.
iDisplay Audio Link Frequency	[48 MHz] <b>[96 MHz]</b>	Selects iDisplay Link frequency.
iDisplay Audio Link T-Mode	[1T Mode] <b>[2T Mode]</b> [4T Mode] [8T Mode] [16T Mode]	Indicates whether SDI is operating in 1T, 2T (CNL).
Autonomous Clock Stop SNDW #0	<b>[Disabled]</b> [Enabled]	Enable/Disable Autonomous Clock Stop for SoundWire LINK0
Autonomous Clock Stop SNDW #1	<b>[Disabled]</b> [Enabled]	Enable/Disable Autonomous Clock Stop for SoundWire LINK1
Autonomous Clock Stop SNDW #2	<b>[Disabled]</b> [Enabled]	Enable/Disable Autonomous Clock Stop for SoundWire LINK2
Autonomous Clock Stop SNDW #3	<b>[Disabled]</b> [Enabled]	Enable/Disable Autonomous Clock Stop for SoundWire LINK3
Autonomous Clock Stop SNDW #4	<b>[Disabled]</b> [Enabled]	Enable/Disable Autonomous Clock Stop for SoundWire LINK4

Data On Active Interval Select SNDW #0	[6 clock periods] [7 clock periods] [8 clock periods] <b>[11 clock periods]</b>	Data On Active Interval Select:\n1) 6 clock periods\n2) 7 clock periods\n3) 8 clock periods\n4) 11 clock periods\n5)
Data On Active Interval Select SNDW #1	[6 clock periods] [7 clock periods] [8 clock periods] <b>[11 clock periods]</b>	Data On Active Interval Select:\n1) 6 clock periods\n2) 7 clock periods\n3) 8 clock periods\n4) 11 clock periods\n5)
Data On Active Interval Select SNDW #2	[6 clock periods] [7 clock periods] [8 clock periods] <b>[11 clock periods]</b>	Data On Active Interval Select:\n1) 6 clock periods\n2) 7 clock periods\n3) 8 clock periods\n4) 11 clock periods\n5)
Data On Active Interval Select SNDW #3	[6 clock periods] [7 clock periods] [8 clock periods] <b>[11 clock periods]</b>	Data On Active Interval Select:\n1) 6 clock periods\n2) 7 clock periods\n3) 8 clock periods\n4) 11 clock periods\n5)
Data On Active Interval Select SNDW #4	[6 clock periods] [7 clock periods] [8 clock periods] <b>[11 clock periods]</b>	Data On Active Interval Select:\n1) 6 clock periods\n2) 7 clock periods\n3) 8 clock periods\n4) 11 clock periods\n5)
Data On Delay Select SNDW #0	[2 clock periods] <b>[3 clock periods]</b>	Data On Delay Select:\n1) 2 clock periods\n2) 3 clock periods\n3)
Data On Delay Select SNDW #1	[2 clock periods] <b>[3 clock periods]</b>	Data On Delay Select:\n1) 2 clock periods\n2) 3 clock periods\n3)
Data On Delay Select SNDW #2	[2 clock periods] <b>[3 clock periods]</b>	Data On Delay Select:\n1) 2 clock periods\n2) 3 clock periods\n3)
Data On Delay Select SNDW #3	[2 clock periods] <b>[3 clock periods]</b>	Data On Delay Select:\n1) 2 clock periods\n2) 3 clock periods\n3)
Data On Delay Select SNDW #4	[2 clock periods] <b>[3 clock periods]</b>	Data On Delay Select:\n1) 2 clock periods\n2) 3 clock periods\n3)

### 2.2.17.5.2 HD Audio DSP Features Configuration

**Table 2-2-17-5-2. HD Audio DSP Features Configuration**

BIOS Setting	Options	Description
HD Audio Subsystem Features Configuration (ACPI)		
<u>(Below options can be set at Audio DSP Compliance Mode set Non-UAA (IntelSST).)</u>		
Audio DSP NHLT Endpoints Configuration:		Audio DSP NHLT Endpoints Configuration:
Dmic Mono 38.4MHz	<b>[Disabled]</b> [Enabled]	Enables/Disables 1 Mic Array Endpoint in NHLT ACPI table. XTAL: 38.4MHz.

Dmic Stereo 38.4MHz	<b>[Disabled]</b> [Enabled]	Enables/Disables 2 Mic Array Endpoint in NHLT ACPI table. XTAL: 38.4MHz.
Dmic Quad 38.4MHz	<b>[Disabled]</b> [Enabled]	Enables/Disables 4 Mic Array Endpoint in NHLT ACPI table. XTAL: 38.4MHz.
Dmic Mono 24MHz	<b>[Disabled]</b> [Enabled]	Enables/Disables 1 Mic Array Endpoint in NHLT ACPI table. XTAL: 2MHz.
Dmic Stereo 24MHz	<b>[Disabled]</b> [Enabled]	Enables/Disables 2 Mic Array Endpoint in NHLT ACPI table. XTAL: 24MHz.
Dmic Quad 24MHz	<b>[Disabled]</b> [Enabled]	Enables/Disables 4 Mic Array Endpoint in NHLT ACPI table. XTAL: 24MHz.
Bluetooth 38.4MHz	<b>[Disabled]</b> [Enabled]	Enables/Disables Bluetooth Endpoint in NHLT ACPI table. XTAL: 38.4MHz.
Bluetooth 24MHz	<b>[Disabled]</b> [Enabled]	Enables/Disables Bluetooth Endpoint in NHLT ACPI table. XTAL: 24MHz.
I2S Alc274 38.4MHz	<b>[Disabled]</b> [Enabled]	Enables/Disables I2S Endpoint for ALC274 in NHLT ACPI table. XTAL: 38.4MHz.
I2S Alc274 24MHz	<b>[Disabled]</b> [Enabled]	Enables/Disables I2S Endpoint for ALC274 in NHLT ACPI table. XTAL: 24MHz.
I2S Codec Select	<b>[Disabled]</b> [Realtek ALC274] [Realtek ALC1308]	Selects I2S Audio Codec support. Note: SerialIo UART0 must be disabled to enable external I2S codec (due to GPIO pin muxing).
I2S Codec Bus Number	<b>[I2C0 Controller]</b> [I2C1 Controller] [I2C2 Controller] [I2C3 Controller] [I2C4 Controller] [I2C5 Controller]	Selects Codec Bus from Serial IO I2C0/1/2/3/4/5
Audio DSP Feature Support:		Enables/Disables DSP Feature. Bitmask structure: [BIT0] - WoV [BIT1] - BT Sideband [BIT2] - Codec based VAD [BIT5] - BT Intel HFP [BIT6] - BT Intel A2DP [BIT7] - DSP based speech pre-processing disabled (for Intel WoV mode)

		[BIT8] - WoV Mode: Intel WoV / Windows Voice Activation for Cortana
WoV (Wake on Voice)	[Disabled] <b>[Enabled]</b>	Enables/Disables DSP Feature. Bitmask structure: [BIT0] - WoV [BIT1] - BT Sideband [BIT2] - Codec based VAD [BIT5] - BT Intel HFP [BIT6] - BT Intel A2DP [BIT7] - DSP based speech pre-processing disabled (for Intel WoV mode) [BIT8] - WoV Mode: Intel WoV / Windows Voice Activation for Cortana
Bluetooth Sideband	<b>[Disabled]</b> [Enabled]	Enables/Disables DSP Feature. Bitmask structure: [BIT0] - WoV [BIT1] - BT Sideband [BIT2] - Codec based VAD [BIT5] - BT Intel HFP [BIT6] - BT Intel A2DP [BIT7] - DSP based speech pre-processing disabled (for Intel WoV mode) <u>[BIT8] - WoV Mode: Intel WoV / Windows Voice Activation for Cortana</u> (Below options can be set at this option set Enabled.)
BT Intel HFP	<b>[Disabled]</b> [Enabled]	Enables/Disables DSP Feature. Bitmask structure: [BIT0] - WoV [BIT1] - BT Sideband [BIT2] - Codec based VAD [BIT5] - BT Intel HFP [BIT6] - BT Intel A2DP [BIT7] - DSP based speech pre-processing disabled (for Intel WoV mode) [BIT8] - WoV Mode: Intel WoV / Windows Voice Activation for Cortana
BT Intel A2DP	<b>[Disabled]</b> [Enabled]	Enables/Disables DSP Feature. Bitmask structure: [BIT0] - WoV [BIT1] - BT Sideband [BIT2] - Codec based VAD [BIT5] - BT Intel HFP [BIT6] - BT Intel A2DP

		<p>[BIT7] - DSP based speech pre-processing disabled (for Intel WoV mode)</p> <p>[BIT8] - WoV Mode: Intel WoV / Windows Voice Activation for Cortana</p>
Codec based VAD	<b>[Disabled]</b> [Enabled]	<p>Enables/Disables DSP Feature. Bitmask structure:</p> <p>[BIT0] - WoV</p> <p>[BIT1] - BT Sideband</p> <p>[BIT2] - Codec based VAD</p> <p>[BIT5] - BT Intel HFP</p> <p>[BIT6] - BT Intel A2DP</p> <p>[BIT7] - DSP based speech pre-processing disabled (for Intel WoV mode)</p> <p>[BIT8] - WoV Mode: Intel WoV / Windows Voice Activation for Cortana</p>
DSP based Speech Pre-Processing Disabled	<b>[Disabled]</b> [Enabled]	<p>Enables/Disables DSP Feature. Bitmask structure:</p> <p>[BIT0] - WoV</p> <p>[BIT1] - BT Sideband</p> <p>[BIT2] - Codec based VAD</p> <p>[BIT5] - BT Intel HFP</p> <p>[BIT6] - BT Intel A2DP</p> <p>[BIT7] - DSP based speech pre-processing disabled (for Intel WoV mode)</p> <p><u>[BIT8] - WoV Mode: Intel WoV / Windows Voice Activation for Cortana</u></p> <p><u>(This option can be set at Voice Activity Detection set Intel Wake on Voice.)</u></p>
Voice Activity Detection	[Intel Wake on Voice] <b>[Windows 10 Voice Activation]</b>	<p>Enables/Disables DSP Feature. Bitmask structure:</p> <p>[BIT0] - WoV</p> <p>[BIT1] - BT Sideband</p> <p>[BIT2] - Codec based VAD</p> <p>[BIT5] - BT Intel HFP</p> <p>[BIT6] - BT Intel A2DP</p> <p>[BIT7] - DSP based speech pre-processing disabled (for Intel WoV mode)</p> <p>[BIT8] - WoV Mode: Intel WoV / Windows Voice Activation for Cortana</p>
Audio DSP Pre/Post-Processing Module Support:		<p>Enables/Disables 3rd Party Processing Module Support (identified by GUID). WoV must be enabled as a feature first to select relevant WoV IP.</p>

Waves Post-process	<b>[Disabled]</b> [Enabled]	Enables/Disables 3rd Party Processing Module Support (identified by GUID). WoV must be enabled as a feature first to select relevant WoV IP.
DTS	<b>[Disabled]</b> [Enabled]	Enables/Disables 3rd Party Processing Module Support (identified by GUID). WoV must be enabled as a feature first to select relevant WoV IP.
IntelSST Speech	<b>[Disabled]</b> [Enabled]	Enables/Disables 3rd Party Processing Module Support (identified by GUID). WoV must be enabled as a feature first to select relevant WoV IP.
Dolby	<b>[Disabled]</b> [Enabled]	Enables/Disables 3rd Party Processing Module Support (identified by GUID). WoV must be enabled as a feature first to select relevant WoV IP.
Waves Pre-process	<b>[Disabled]</b> [Enabled]	Enables/Disables 3rd Party Processing Module Support (identified by GUID). WoV must be enabled as a feature first to select relevant WoV IP.
Audyssey	<b>[Disabled]</b> [Enabled]	Enables/Disables 3rd Party Processing Module Support (identified by GUID). WoV must be enabled as a feature first to select relevant WoV IP.
Maxim Smart AMP	<b>[Disabled]</b> [Enabled]	Enables/Disables 3rd Party Processing Module Support (identified by GUID). WoV must be enabled as a feature first to select relevant WoV IP.
ForteMedia SAMSoft	<b>[Disabled]</b> [Enabled]	Enables/Disables 3rd Party Processing Module Support (identified by GUID). WoV must be enabled as a feature first to select relevant WoV IP.
Sound Research IP	<b>[Disabled]</b> [Enabled]	Enables/Disables 3rd Party Processing Module Support (identified by GUID). WoV must be enabled as a feature first to select relevant WoV IP.
Conexant Pre-Process	<b>[Disabled]</b> [Enabled]	Enables/Disables 3rd Party Processing Module Support (identified by GUID). WoV must be enabled as a feature first to select relevant WoV IP.

Conexant Smart Amp	<b>[Disabled]</b> [Enabled]	Enables/Disables 3rd Party Processing Module Support (identified by GUID). WoV must be enabled as a feature first to select relevant WoV IP.
Realtek Post-Process	<b>[Disabled]</b> [Enabled]	Enables/Disables 3rd Party Processing Module Support (identified by GUID). WoV must be enabled as a feature first to select relevant WoV IP.
Realtek Smart Amp	<b>[Disabled]</b> [Enabled]	Enables/Disables 3rd Party Processing Module Support (identified by GUID). WoV must be enabled as a feature first to select relevant WoV IP.
Icepower IP MFX sub module	<b>[Disabled]</b> [Enabled]	Enables/Disables 3rd Party Processing Module Support (identified by GUID). WoV must be enabled as a feature first to select relevant WoV IP.
Icepower IP EFX sub module	<b>[Disabled]</b> [Enabled]	Enables/Disables 3rd Party Processing Module Support (identified by GUID). WoV must be enabled as a feature first to select relevant WoV IP.
Icepower IP SFX sub module	<b>[Disabled]</b> [Enabled]	Enables/Disables 3rd Party Processing Module Support (identified by GUID). WoV must be enabled as a feature first to select relevant WoV IP.
Voice Preprocessing	<b>[Disabled]</b> [Enabled]	Enables/Disables 3rd Party Processing Module Support (identified by GUID). WoV must be enabled as a feature first to select relevant WoV IP.
Acoustic Context Awareness (ACA)	<b>[Disabled]</b> [Enabled]	Enables/Disables 3rd Party Processing Module Support (identified by GUID). WoV must be enabled as a feature first to select relevant WoV IP.
Custom Module 'Alpha'	<b>[Disabled]</b> [Enabled]	Enables/Disables 3rd Party Processing Module Support (identified by GUID). WoV must be enabled as a feature first to select relevant WoV IP.
'Alpha' GUID:	<b>minsize = 36</b> <b>maxsize = 36</b>	Input hex digit character in aabbccdd-eeff-gghh-ijjj-kklmmnoopp format. <u>(This option will show at Custom Module 'Alpha' set Enabled.)</u>

Custom Module 'Beta'	<b>[Disabled]</b> [Enabled]	Enables/Disables 3rd Party Processing Module Support (identified by GUID). WoV must be enabled as a feature first to select relevant WoV IP.
'Beta' GUID:	<b>minsize = 36</b> <b>maxsize = 36</b>	Input hex digit character in aabbccdd-eeff-gghh-ijjj-kkllmmnnnoopp format. <u>(This option will show at Custom Module 'Beta' set Enabled.)</u>
Custom Module 'Gamma'	<b>[Disabled]</b> [Enabled]	Enables/Disables 3rd Party Processing Module Support (identified by GUID). WoV must be enabled as a feature first to select relevant WoV IP.
'Gamma' GUID:	<b>minsize = 36</b> <b>maxsize = 36</b>	Input hex digit character in aabbccdd-eeff-gghh-ijjj-kkllmmnnnoopp format. <u>(This option will show at Custom Module 'Gamma' set Enabled.)</u>

### 2.2.17.6 THC Configuration

**Table 2-2-17-6. THC Configuration**

BIOS Setting	Options	Description
SerialIo Configuration		
THC Port Configuration	<b>[None]</b> [THC0]	Assign Port to THC <i>(Below will show at this set THC0)</i>
Wake On Touch	<b>[Disabled]</b> [Enabled]	Based on this setting vGPIO for given THC will be in native mode, and additional _CRS for wake will be exposed in ACPI
Port Clock	<b>[Functional]</b> [DFX]	SPI_DFX_CLK_EN BIT set to 0 or 1
THC Port Configuration	<b>[None]</b> [THC1]	Assign Port to THC <i>(Below will show at this set THC1)</i>
Wake On Touch	<b>[Disabled]</b> [Enabled]	Based on this setting vGPIO for given THC will be in native mode, and additional _CRS for wake will be exposed in ACPI
Port Clock	<b>[Functional]</b> [DFX]	SPI_DFX_CLK_EN BIT set to 0 or 1

### 2.2.17.7 Serial IO Configuration

**Table 2-2-17-7. Serial IO Configuration**

BIOS Setting	Options	Description
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SerialIo Configuration		
I2C0 Controller	[Disabled] <b>[Enabled]</b>	<p>Enables/Disables SerialIo Controller            If given device is Function 0 PSF disabling is skipped. PSF default will remain and device PCI CFG Space will still be visible. This is needed to allow PCI enumerator access functions above 0 in a multifunction device.            The following devices depend on each other:            I2C0 and I2C1,2,3            UART0 and UART1,SPI0,1            UART2 and I2C4,5            UART 0 (00:30:00) cannot be disabled when:            1. Child device is enabled like CNVi Bluetooth (\_SB.PCI0.UA00.BTH0)            UART 0 (00:30:00) cannot be enabled when:            1. I2S Audio codec is enabled (\_SB.PCI0.I2C0.HDAC)</p>
I2C1 Controller	[Disabled] <b>[Enabled]</b>	<p>Enables/Disables SerialIo Controller            If given device is Function 0 PSF disabling is skipped. PSF default will remain and device PCI CFG Space will still be visible. This is needed to allow PCI enumerator access functions above 0 in a multifunction device.            The following devices depend on each other:            I2C0 and I2C1,2,3            UART0 and UART1,SPI0,1            UART2 and I2C4,5            UART 0 (00:30:00) cannot be disabled when:            1. Child device is enabled like CNVi Bluetooth (\_SB.PCI0.UA00.BTH0)            UART 0 (00:30:00) cannot be enabled when:            1. I2S Audio codec is enabled (\_SB.PCI0.I2C0.HDAC)</p>
I2C2 Controller	<b>[Disabled]</b> [Enabled]	<p>Enables/Disables SerialIo Controller            If given device is Function 0 PSF disabling is skipped. PSF default will remain and device PCI CFG Space will still be visible. This is needed to allow PCI enumerator access functions above 0 in a multifunction device.            The following devices depend on each other:            I2C0 and I2C1,2,3            UART0 and UART1,SPI0,1            UART2 and I2C4,5</p>

		<p>UART 0 (00:30:00) cannot be disabled when:</p> <ol style="list-style-type: none"> <li>1. Child device is enabled like CNVi Bluetooth (\_SB.PCI0.UA00.BTH0)</li> </ol> <p>UART 0 (00:30:00) cannot be enabled when:</p> <ol style="list-style-type: none"> <li>1. I2S Audio codec is enabled (\_SB.PCI0.I2C0.HDAC)</li> </ol>
I2C3 Controller	<b>[Disabled]</b> [Enabled]	<p>Enables/Disables SerialIo Controller</p> <p>If given device is Function 0 PSF disabling is skipped. PSF default will remain and device PCI CFG Space will still be visible. This is needed to allow PCI enumerator access functions above 0 in a multifunction device. The following devices depend on each other:</p> <p>I2C0 and I2C1,2,3          UART0 and UART1,SPI0,1          UART2 and I2C4,5</p> <p>UART 0 (00:30:00) cannot be disabled when:</p> <ol style="list-style-type: none"> <li>1. Child device is enabled like CNVi Bluetooth (\_SB.PCI0.UA00.BTH0)</li> </ol> <p>UART 0 (00:30:00) cannot be enabled when:</p> <ol style="list-style-type: none"> <li>1. I2S Audio codec is enabled (\_SB.PCI0.I2C0.HDAC)</li> </ol>
I2C4 Controller	<b>[Disabled]</b> [Enabled]	<p>Enables/Disables SerialIo Controller</p> <p>For I2C5 and UART2 to work this device has to be enabled</p> <p>(Show as <u>SETUP_VOLATILE_DATA.PlatformType</u> is TypeUltUlx)</p>
I2C5 Controller	[Disabled] <b>[Enabled]</b>	<p>Enables/Disables SerialIo Controller</p> <p>For this device to work I2C4 has to be enabled</p> <p>(Show as <u>SETUP_VOLATILE_DATA.PlatformType</u> is TypeUltUlx)</p>
I2C6 Controller	<b>[Disabled]</b> [Enabled]	<p>Enables/Disables SerialIo Controller</p> <p>If given device is Function 0 PSF disabling is skipped. PSF default will remain and device PCI CFG Space will still be visible. This is needed to allow PCI enumerator access functions above 0 in a multifunction device. The following devices depend on each other:</p> <p>I2C0 and I2C1,2,3          UART0 and UART1,SPI0,1          UART2 and I2C4,5</p>

		<p>UART 0 (00:30:00) cannot be disabled when:</p> <ol style="list-style-type: none"> <li>1. Child device is enabled like CNVi Bluetooth (\_SB.PCI0.UA00.BTH0)</li> </ol> <p>UART 0 (00:30:00) cannot be enabled when:</p> <ol style="list-style-type: none"> <li>1. I2S Audio codec is enabled (\_SB.PCI0.I2C0.HDAC)</li> </ol>
I2C7 Controller	<b>[Disabled]</b> [Enabled]	<p>Enables/Disables SerialIo Controller. If given device is Function 0 PSF disabling is skipped. PSF default will remain and device PCI CFG Space will still be visible. This is needed to allow PCI enumerator access functions above 0 in a multifunction device. The following devices depend on each other:</p> <p>I2C0 and I2C1,2,3            UART0 and UART1,SPI0,1            UART2 and I2C4,5</p> <p>UART 0 (00:30:00) cannot be disabled when:</p> <ol style="list-style-type: none"> <li>1. Child device is enabled like CNVi Bluetooth (\_SB.PCI0.UA00.BTH0)</li> </ol> <p>UART 0 (00:30:00) cannot be enabled when:</p> <ol style="list-style-type: none"> <li>1. I2S Audio codec is enabled (\_SB.PCI0.I2C0.HDAC)</li> </ol>
SPI0 Controller	<b>[Disabled]</b> [Enabled]	<p>Enables/Disables SerialIo Controller. If given device is Function 0 PSF disabling is skipped. PSF default will remain and device PCI CFG Space will still be visible. This is needed to allow PCI enumerator access functions above 0 in a multifunction device. The following devices depend on each other:</p> <p>I2C0 and I2C1,2,3            UART0 and UART1,SPI0,1            UART2 and I2C4,5</p> <p>UART 0 (00:30:00) cannot be disabled when:</p> <ol style="list-style-type: none"> <li>1. Child device is enabled like CNVi Bluetooth (\_SB.PCI0.UA00.BTH0)</li> </ol> <p>UART 0 (00:30:00) cannot be enabled when:</p> <ol style="list-style-type: none"> <li>1. I2S Audio codec is enabled (\_SB.PCI0.I2C0.HDAC)</li> </ol>
SPI1 Controller	[Disabled] <b>[Enabled]</b>	<p>Enables/Disables SerialIo Controller. If given device is Function 0 PSF disabling is skipped. PSF default will remain and device PCI CFG Space will still be visible. This is needed to allow</p>

		<p>PCI enumerator access functions above 0 in a multifunction device. The following devices depend on each other:</p> <p>I2C0 and I2C1,2,3            UART0 and UART1,SPI0,1            UART2 and I2C4,5            UART 0 (00:30:00) cannot be disabled when:</p> <ol style="list-style-type: none"> <li>Child device is enabled like CNVi Bluetooth (\_SB.PCI0.UA00.BTH0)</li> </ol> <p>UART 0 (00:30:00) cannot be enabled when:</p> <ol style="list-style-type: none"> <li>I2S Audio codec is enabled (\_SB.PCI0.I2C0.HDAC)</li> </ol>
SPI2 Controller	<b>[Disabled]</b> [Enabled]	<p>Enables/Disables SerialIo SPI2 Controller</p> <p>The following device depends from: Thermal Subsystem in PCI mode</p> <p>Otherwise SPI2 will not appear in the OS</p>
SPI3 Controller	[Disabled] <b>[Enabled]</b>	<p>Enables/Disables SerialIo Controller</p> <p>If given device is Function 0 PSF disabling is skipped. PSF default will remain and device PCI CFG Space will still be visible. This is needed to allow PCI enumerator access functions above 0 in a multifunction device. The following devices depend on each other:</p> <p>I2C0 and I2C1,2,3            UART0 and UART1,SPI0,1            UART2 and I2C4,5            UART 0 (00:30:00) cannot be disabled when:</p> <ol style="list-style-type: none"> <li>Child device is enabled like CNVi Bluetooth (\_SB.PCI0.UA00.BTH0)</li> </ol> <p>UART 0 (00:30:00) cannot be enabled when:</p> <ol style="list-style-type: none"> <li>I2S Audio codec is enabled (\_SB.PCI0.I2C0.HDAC)</li> </ol>
SPI4 Controller	[Disabled] <b>[Enabled]</b>	<p>Enables/Disables SerialIo Controller</p> <p>If given device is Function 0 PSF disabling is skipped. PSF default will remain and device PCI CFG Space will still be visible. This is needed to allow PCI enumerator access functions above 0 in a multifunction device. The following devices depend on each other:</p> <p>I2C0 and I2C1,2,3            UART0 and UART1,SPI0,1            UART2 and I2C4,5</p>

		<p>UART 0 (00:30:00) cannot be disabled when:</p> <ol style="list-style-type: none"> <li>Child device is enabled like CNVi Bluetooth (\_SB.PCI0.UA00.BTH0)</li> </ol> <p>UART 0 (00:30:00) cannot be enabled when:</p> <ol style="list-style-type: none"> <li>I2S Audio codec is enabled (\_SB.PCI0.I2C0.HDAC)</li> </ol>
SPI5 Controller	[Disabled] <b>[Enabled]</b>	<p>Enables/Disables SerialIo Controller. If given device is Function 0 PSF disabling is skipped. PSF default will remain and device PCI CFG Space will still be visible. This is needed to allow PCI enumerator access functions above 0 in a multifunction device. The following devices depend on each other:</p> <p>I2C0 and I2C1,2,3          UART0 and UART1,SPI0,1          UART2 and I2C4,5</p> <p>UART 0 (00:30:00) cannot be disabled when:</p> <ol style="list-style-type: none"> <li>Child device is enabled like CNVi Bluetooth (\_SB.PCI0.UA00.BTH0)</li> </ol> <p>UART 0 (00:30:00) cannot be enabled when:</p> <ol style="list-style-type: none"> <li>I2S Audio codec is enabled (\_SB.PCI0.I2C0.HDAC)</li> </ol>
SPI6 Controller	[Disabled] <b>[Enabled]</b>	<p>Enables/Disables SerialIo Controller. If given device is Function 0 PSF disabling is skipped. PSF default will remain and device PCI CFG Space will still be visible. This is needed to allow PCI enumerator access functions above 0 in a multifunction device. The following devices depend on each other:</p> <p>I2C0 and I2C1,2,3          UART0 and UART1,SPI0,1          UART2 and I2C4,5</p> <p>UART 0 (00:30:00) cannot be disabled when:</p> <ol style="list-style-type: none"> <li>Child device is enabled like CNVi Bluetooth (\_SB.PCI0.UA00.BTH0)</li> </ol> <p>UART 0 (00:30:00) cannot be enabled when:</p> <ol style="list-style-type: none"> <li>I2S Audio codec is enabled (\_SB.PCI0.I2C0.HDAC)</li> </ol>
UART0 Controller	<b>[Disabled]</b> [Enabled] [Communication port (COM)]	<p>Enables/Disables SerialIo Controller. If given device is Function 0 PSF disabling is skipped. PSF default will remain and device PCI CFG Space will still be visible. This is needed to allow</p>

		<p>PCI enumerator access functions above 0 in a multifunction device. The following devices depend on each other:</p> <p>I2C0 and I2C1,2,3          UART0 and UART1,SPI0,1          UART2 and I2C4,5          UART 0 (00:30:00) cannot be disabled when:</p> <ol style="list-style-type: none"> <li>Child device is enabled like CNVi Bluetooth (\_SB.PCI0.UA00.BTH0)</li> </ol> <p>UART 0 (00:30:00) cannot be enabled when:</p> <ol style="list-style-type: none"> <li>I2S Audio codec is enabled (\_SB.PCI0.I2C0.HDAC)</li> </ol> <p><u>(This option can be set at I2S Codec Select set Disabled.)</u></p>
UART1 Controller	<p><b>[Disabled]</b>          [Enabled]          [Communication port (COM)]</p>	<p>Enables/Disables SerialIo Controller          If given device is Function 0 PSF disabling is skipped. PSF default will remain and device PCI CFG Space will still be visible. This is needed to allow PCI enumerator access functions above 0 in a multifunction device. The following devices depend on each other:</p> <p>I2C0 and I2C1,2,3          UART0 and UART1,SPI0,1          UART2 and I2C4,5          UART 0 (00:30:00) cannot be disabled when:</p> <ol style="list-style-type: none"> <li>Child device is enabled like CNVi Bluetooth (\_SB.PCI0.UA00.BTH0)</li> </ol> <p>UART 0 (00:30:00) cannot be enabled when:</p> <ol style="list-style-type: none"> <li>I2S Audio codec is enabled (\_SB.PCI0.I2C0.HDAC)</li> </ol>
UART2 Controller	<p>MDEPKG_NDEBUG is defined:  <b>[Disabled]</b>          [Enabled]          [Communication port (COM)]</p> <p>else:  <b>[for debug only]</b>          [Enabled]</p>	<p>Set UART2 mode</p> <ul style="list-style-type: none"> <li>- DBG used for BIOS log print and/or Kernel OS Debug</li> <li>- COM - 16550 compatible serial port with Power Gating support</li> </ul> <p><u>(This option can be set at Kernel Debug Serial Port set Legacy UART.)</u></p>
GPIO IRQ Route	<b>[IRQ14]</b> [IRQ15]	Route all GPIOs to one of the IRQ.
Serial IO I2C0 Settings	(See Section 2.2.17.7.1)	Configure SerialIo Controller <u>(This option will show at I2C0 Controller set Enabled.)</u>
Serial IO I2C1 Settings	(See Section 2.2.17.7.1)	Configure SerialIo Controller <u>(This option will show at I2C1 Controller set Enabled.)</u>

Serial IO I2C2 Settings	(See Section 2.2.17.7.1)	Configure SerialIo Controller (This option will show at I2C2 Controller set Enabled.)
Serial IO I2C3 Settings	(See Section 2.2.17.7.1)	Configure SerialIo Controller (This option will show at I2C3 Controller set Enabled.)
Serial IO I2C4 Settings	(See Section 2.2.17.7.2)	Configure SerialIo Controller (This option will show at I2C4 Controller set Enabled.)
Serial IO I2C5 Settings	(See Section 2.2.17.7.2)	Configure SerialIo Controller (This option will show at I2C5 Controller set Enabled.)
Serial IO SPI0 Settings	(See Section 2.2.17.7.3)	Configure SerialIo Controller (This option will show at SPI0 set Enabled.)
Serial IO SPI1 Settings	(See Section 2.2.17.7.4)	Configure SerialIo Controller (This option will show at SPI1 set Enabled.)
Serial IO SPI2 Settings	(See Section 2.2.17.7.4)	Configure SerialIo Controller (This option will show at SPI2 set Enabled.)
Serial IO UART0 Settings	(See Section 2.2.17.7.5)	Configure SerialIo Controller (This option will show at UART0 Controller set Enabled.)
Serial IO UART1 Settings	(See Section 2.2.17.7.5)	Configure SerialIo Controller (This option will show at UART1 Controller set Enabled.)
Serial IO UART2 Settings	(See Section 2.2.17.7.5)	Configure SerialIo Controller (This option will show at UART2 Controller set Enabled.)
WITT/MITT Test Device	<b>[Disabled]</b> [Enabled - I2C0] [Enabled - I2C1] [Enabled - I2C2] [Enabled - I2C3] [Enabled - I2C4] [Enabled - I2C5] [Enabled - SPI0] [Enabled - SPI1] [Enabled - SPI2]	Choose if WITT Device is used and with which controller (Below option will show at this option set Enabled.)
WITT/MITT Device selection	[WITT] <b>[MITT]</b>	Change WITT Device version
UART Test Device	<b>[Disabled]</b> [Enabled - UART0] [Enabled - UART1] [Enabled - UART2]	Choose if UART Test Device is used and with which controller
Additional Serial IO devices	<b>[Disabled]</b> [Enabled]	When enabled, ACPI will report additional devices connected to Serial IO.
SerialIO timing parameters	<b>[Disabled]</b> [Enabled]	Enables additional timing parameters for all SerialIO controllers.

		Defaults can be changed in each controller setting. Platform restart required to apply changes
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### 2.2.17.7.1 Serial IO I2C0/I2C1/I2C2/I2C3 Settings

Table 2-2-17-7-1. Serial IO I2C0/I2C1/I2C2/I2C3 Settings

BIOS Setting	Options	Description
Serial IO I2C# Settings		
Serial IO Touch Pad Settings	(See Section 2.2.17.7.1.1)	Indicates what type of I2C Touch Pad is connected to this SerialIo controller (Show as <u>SETUP_DATA.PchI2cSensorDevicePort[SERIAL_IO_I2C0]</u> is not 1 3 5 7; ) //Please refer "8 Bits Map of I2C Devices" in SetupVariable.h
Serial IO Touch Panel Settings	(See Section 2.2.17.7.1.2)	Indicates what type of I2C Touch Panel is connected to this SerialIo controller (Show as <u>SETUP_DATA.PchI2cSensorDevicePort[SERIAL_IO_I2C0]</u> is not 2 3 6 7; ) //Please refer "8 Bits Map of I2C Devices" in SetupVariable.h
(Below options will show at SerialIO timing parameters set Enabled.)		
Timing parameters		
StandardSpeed SCL High	<b>minimum = 0</b> <b>maximum = 65535</b> <b>default = 1010</b>	Default: 1010 [DEC] Minimum: 1 [DEC] Maximum: 65535 [DEC]
StandardSpeed SCL Low	<b>minimum = 0</b> <b>maximum = 65535</b> <b>default = 1085</b>	Default: 1085 [DEC] Minimum: 1 [DEC] Maximum: 65535 [DEC]
StandardSpeed SDA Hold	<b>minimum = 0</b> <b>maximum = 65535</b> <b>default = 28</b>	Default: 28 [DEC] Minimum: 1 [DEC] Maximum: 65535 [DEC]
FastSpeed SCL High	<b>minimum = 0</b> <b>maximum = 65535</b> <b>default = 193</b>	Default: 193 [DEC] Minimum: 1 [DEC] Maximum: 65535 [DEC]
FastSpeed SCL Low	<b>minimum = 0</b> <b>maximum = 65535</b>	Default: 313 [DEC] Minimum:

	<b>default = 313</b>	1 [DEC] Maximum: 65535 [DEC]
FastSpeed SDA Hold	<b>minimum = 0</b> <b>maximum = 65535</b> <b>default = 30</b>	Default: 30 [DEC] Minimum: 1 [DEC] Maximum: 65535 [DEC]
FastSpeedPlus SCL High	<b>minimum = 0</b> <b>maximum = 65535</b> <b>default = 61</b>	Default: 61 [DEC] Minimum: 1 [DEC] Maximum: 65535 [DEC]
FastSpeedPlus SCL Low	<b>minimum = 0</b> <b>maximum = 65535</b> <b>default = 132</b>	Default: 132 [DEC] Minimum: 1 [DEC] Maximum: 65535 [DEC]
FastSpeedPlus SDA Hold	<b>minimum = 0</b> <b>maximum = 65535</b> <b>default = 30</b>	Default: 30 [DEC] Minimum: 1 [DEC] Maximum: 65535 [DEC]
HighSpeed SCL High	<b>minimum = 0</b> <b>maximum = 65535</b> <b>default = 11</b>	Default: 11 [DEC] Minimum: 1 [DEC] Maximum: 65535 [DEC]
HighSpeed SCL Low	<b>minimum = 0</b> <b>maximum = 65535</b> <b>default = 19</b>	Default: 19 [DEC] Minimum: 1 [DEC] Maximum: 65535 [DEC]
HighSpeed SDA Hold	<b>minimum = 0</b> <b>maximum = 65535</b> <b>default = 30</b>	Default: 30 [DEC] Minimum: 1 [DEC] Maximum: 65535 [DEC]
D0->D3 idle timeout (screen off)	<b>minimum = 1</b> <b>maximum = 10000</b> <b>default = 200</b>	Default: 200 [DEC] Minimum: 1 [DEC] Maximum: 10000 [DEC]

D0->D3 idle timeout (screen on)	<b>minimum = 1</b> <b>maximum = 10000</b> <b>default = 2000</b>	Default: 2000 [DEC] Minimum: 1 [DEC] Maximum: 10000 [DEC]
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### 2.2.17.7.1.1 Serial IO Touch Pad Settings

**Table 2-2-17-7-1-1. Serial IO Touch Pad Settings**

BIOS Setting	Options	Description
Touch Pad	<b>[Disabled]</b> [Synaptics Precision Touchpad] [Synaptics Forcepad] [ALPS Precision Touchpad ClickPad] [Custom device]	Indicates what type of I2C Touch Pad is connected to this SerialIo controller
Touch Pad Interrupt Mode	[GPIO Interrupt] <b>[APIC Interrupt]</b>	Selects different routing for interrupts from Touch Pad (This option will show at Touch Pad set Enabled.)
(Below options will show at Touch Pad set Custom device.)		
Device's bus address	<b>minimum = 0</b> <b>maximum = 0x7F</b> <b>step = 1</b> <b>default = 0</b>	Specify parameters of custom I2C device
Device's HID address	<b>minimum = 0</b> <b>maximum = 0xFFFF</b> <b>step = 1</b> <b>default = 0</b>	Specify parameters of custom I2C device
Device's bus speed	<b>[100kHz]</b> [400kHz] [1MHz]	Specify parameters of custom I2C device

### 2.2.17.7.1.2 Serial IO Touch Panel Settings

**Table 2-2-17-7-1-2. Serial IO Touch Panel Settings**

BIOS Setting	Options	Description
Touch Panel	<b>[Disabled]</b> [Atmel3432 TouchPanel] [Atmel2952 TouchPanel] [Elan2097 TouchPanel] [N-Trig/Samsung 13.3\ [N-Trig/Sharp 12.5\ [WACOM TouchPanel] [Custom device]	Indicates what type of I2C Touch Panel is connected to this SerialIo controller
Touch Panel Interrupt Mode	[GPIO Interrupt] <b>[APIC Interrupt]</b>	Selects different routing for interrupts from Touch Panel

		(This option will show at Touch Panel set Enabled.)
(Below options will show at Touch Panel set Custom device.)		
Device's bus address	<b>minimum = 0</b> <b>maximum = 0x7F</b> <b>step = 1</b> <b>default = 0</b>	Specify parameters of custom I2C device
Device's HID address	<b>minimum = 0</b> <b>maximum = 0xFFFF</b> <b>step = 1</b> <b>default = 0</b>	Specify parameters of custom I2C device
(Below option will show at Touch Panel set WACOM TouchPanel or Custom device.)		
Device's bus speed	[100kHz] <b>[400kHz]</b> [1MHz]	Specify parameters of custom I2C device

### 2.2.17.7.2 Serial IO I2C4/ I2C5 Settings

**Table 2-2-17-7-2. Serial IO I2C4/I2C5 Settings**

BIOS Setting	Options	Description
Serial IO I2C# Settings		
(Below options will show at SerialIO timing parameters set Enabled.)		
Timing parameters		
StandardSpeed SCL High	<b>minimum = 0</b> <b>maximum = 65535</b> <b>default = 1010</b>	Default: 1010 [DEC] Minimum: 1 [DEC] Maximum: 65535 [DEC]
StandardSpeed SCL Low	<b>minimum = 0</b> <b>maximum = 65535</b> <b>default = 1085</b>	Default: 1085 [DEC] Minimum: 1 [DEC] Maximum: 65535 [DEC]
StandardSpeed SDA Hold	<b>minimum = 0</b> <b>maximum = 65535</b> <b>default = 28</b>	Default: 28 [DEC] Minimum: 1 [DEC] Maximum: 65535 [DEC]
FastSpeed SCL High	<b>minimum = 0</b> <b>maximum = 65535</b> <b>default = 193</b>	Default: 193 [DEC] Minimum: 1 [DEC] Maximum:

		65535 [DEC]
FastSpeed SCL Low	<b>minimum = 0</b> <b>maximum = 65535</b> <b>default = 313</b>	Default: 313 [DEC] Minimum: 1 [DEC] Maximum: 65535 [DEC]
FastSpeed SDA Hold	<b>minimum = 0</b> <b>maximum = 65535</b> <b>default = 30</b>	Default: 30 [DEC] Minimum: 1 [DEC] Maximum: 65535 [DEC]
FastSpeedPlus SCL High	<b>minimum = 0</b> <b>maximum = 65535</b> <b>default = 61</b>	Default: 61 [DEC] Minimum: 1 [DEC] Maximum: 65535 [DEC]
FastSpeedPlus SCL Low	<b>minimum = 0</b> <b>maximum = 65535</b> <b>default = 132</b>	Default: 132 [DEC] Minimum: 1 [DEC] Maximum: 65535 [DEC]
FastSpeedPlus SDA Hold	<b>minimum = 0</b> <b>maximum = 65535</b> <b>default = 30</b>	Default: 30 [DEC] Minimum: 1 [DEC] Maximum: 65535 [DEC]
HighSpeed SCL High	<b>minimum = 0</b> <b>maximum = 65535</b> <b>default = 11</b>	Default: 11 [DEC] Minimum: 1 [DEC] Maximum: 65535 [DEC]
HighSpeed SCL Low	<b>minimum = 0</b> <b>maximum = 65535</b> <b>default = 19</b>	Default: 19 [DEC] Minimum: 1 [DEC] Maximum: 65535 [DEC]
HighSpeed SDA Hold	<b>minimum = 0</b> <b>maximum = 65535</b> <b>default = 30</b>	Default: 30 [DEC] Minimum: 1 [DEC] Maximum: 65535 [DEC]

D0->D3 idle timeout (screen off)	<b>minimum = 1</b> <b>maximum = 10000</b> <b>default = 200</b>	Default: 200 [DEC] Minimum: 1 [DEC] Maximum: 10000 [DEC]
D0->D3 idle timeout (screen on)	<b>minimum = 1</b> <b>maximum = 10000</b> <b>default = 2000</b>	Default: 2000 [DEC] Minimum: 1 [DEC] Maximum: 10000 [DEC]

### 2.2.17.7.3 Serial IO SPI0 Settings

**Table 2-2-17-7-3. Serial IO SPI0 Settings**

BIOS Setting	Options	Description
Serial IO SPI0 Settings		
ChipSelect 0 polarity	[Active Low] <b>[Active High]</b>	Sets initial polarity for ChipSelect signal
ChipSelect 1 polarity	[Active Low] <b>[Active High]</b>	Sets initial polarity for ChipSelect signal
(Below options will show at SerialIO timing parameters set Enabled.)		
Timing parameters		
D0->D3 idle timeout (screen off)	<b>minimum = 1</b> <b>maximum = 10000</b> <b>default = 200</b>	Default: 200 [DEC] Minimum: 1 [DEC] Maximum: 10000 [DEC]
D0->D3 idle timeout (screen on)	<b>minimum = 1</b> <b>maximum = 10000</b> <b>default = 2000</b>	Default: 2000 [DEC] Minimum: 1 [DEC] Maximum: 10000 [DEC]

### 2.2.17.7.4 Serial IO SPI1/SPI2 Settings

**Table 2-2-17-7-4. Serial IO SPI1/SPI2 Settings**

BIOS Setting	Options	Description
Serial IO SPI# Settings		
ChipSelect 0 polarity	[Active Low] <b>[Active High]</b>	Sets initial polarity for ChipSelect signal
ChipSelect 1 polarity	[Active Low] <b>[Active High]</b>	Sets initial polarity for ChipSelect signal

Serial IO Finger Print Settings	(See Section 2.2.16.6.4.1)	Select the HID to enable Finger Print Sensor
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### 2.2.17.7.4.1 Serial IO Finger Print Settings

**Table 2-2-17-7-4-1. Serial IO Finger Print Settings**

BIOS Setting	Options	Description
Finger Print Sensor	<b>[Disabled]</b> [FPC1011] [FPC1020] [VFSI6101] [Synaptics VFSI7500] [EGIS0300] [FPC1021]	Select the HID to enable Finger Print Sensor
Finger Print Interrupt Mode	[GPIO Interrupt] <b>[APIC Interrup]</b>	Selects different routing for interrupts from Finger Print (This option will show at Finger Print Sensor set Enabled.)
(Below options will show at SerialIO timing parameters set Enabled.)		
Timing parameters		
D0->D3 idle timeout (screen off)	<b>minimum = 1</b> <b>maximum = 10000</b> <b>default = 200</b>	Default: 200 [DEC] Minimum: 1 [DEC] Maximum: 10000 [DEC]
D0->D3 idle timeout (screen on)	<b>minimum = 1</b> <b>maximum = 10000</b> <b>default = 2000</b>	Default: 2000 [DEC] Minimum: 1 [DEC] Maximum: 10000 [DEC]
Timing parameters		
D0->D3 idle timeout (screen off)	<b>minimum = 1</b> <b>maximum = 10000</b> <b>default = 200</b>	Default: 200 [DEC] Minimum: 1 [DEC] Maximum: 10000 [DEC]
D0->D3 idle timeout (screen on)	<b>minimum = 1</b> <b>maximum = 10000</b> <b>default = 2000</b>	Default: 2000 [DEC] Minimum: 1 [DEC] Maximum: 10000 [DEC]

### 2.2.17.7.5 Serial IO UART0/UART1/UAT2 Settings

**Table 2-2-17-7-5. Serial IO UART0/UART1/UART2 Settings**

BIOS Setting	Options	Description
Serial IO UART# Settings		
Hardware Flow Control	[Disabled] <b>[Enabled]</b>	When enabled configures additional 2 GPIO pads for use as RTS/CTS signals for UART
DMA Enable	[Disabled] <b>[Enabled]</b>	Enabled: UART OS driver will use DMA when possible. Disabled: OS driver will enforce PIO mode
Power Gating	[Disabled] [Enabled] <b>[Auto]</b>	Disabled: No _PS0 _PS3 support, device is left in D0, after initialization Enabled: _PS0 _PS3 that supports getting device out of reset Auto: _PS0 and _PS3 detection through ACPI if device was initialized prior to first PG. If it was used (DBG2) PG is disabled (This option will show at <u>UART0/UART1/UART2 Controller set Communication port (COM)</u> )
(Below options will show at SerialIO timing parameters set Enabled.)		
Timing parameters		
D0->D3 idle timeout (screen off)	<b>minimum = 1</b> <b>maximum = 10000</b> <b>default = 200</b>	Default: 200 [DEC] Minimum: 1 [DEC] Maximum: 10000 [DEC]
D0->D3 idle timeout (screen on)	<b>minimum = 1</b> <b>maximum = 10000</b> <b>default = 200</b>	Default: 200 [DEC] Minimum: 1 [DEC] Maximum: 10000 [DEC]

### 2.2.17.8 SCS Configuration

**Table 2-2-17-8. SCS Configuration**

BIOS Setting	Options	Description
SDCard 3.0 Controller	[Disabled] <b>[Enabled]</b>	Enable or Disable SCS SDHC 3.0 Controller

UFS 2.0 Controller	EMBEDDED_FLAG is defined: <b>[Disabled]</b> [Enabled]  else: [Disabled] <b>[Enabled]</b>	Enable or Disable UFS 2.0 Controller
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### 2.2.17.9 ISH Configuration

**Table 2-2-17-9. ISH Configuration**

BIOS Setting	Options	Description
ISH Controller	[Disabled] <b>[Enabled]</b>	Enables/Disables Integrated Sensor Hub (ISH) Device (Below options will show at this option set Enabled.)
PDT Unlock Message	<b>[Disabled]</b> [Enabled]	Checked = Sends PDT Unlock Message to ISH. After the message is sent the field is set back to unchecked automatically.
ISH GPIO Assignment Configuration		Checked = Pin set to ISH Native function. Checkbox grayed out = disable conflicting SerialIo controller to set. Shared pins: 1. ISH UART0 - LPSS I2C2(PCH-H) 2. ISH UART1 - LPSS UART1 3. ISH I2C2 - LPSS I2C5(PCH-LP) / I2C3(PCH-H)
SPI_0	<b>[Disabled]</b> [Enabled]	Checked = Pin set to ISH Native function. Checkbox grayed out = disable conflicting SerialIo controller to set. Shared pins: 1. ISH UART0 - LPSS I2C2(PCH-H) 2. ISH UART1 - LPSS UART1 3. ISH I2C2 - LPSS I2C5(PCH-LP) / I2C3(PCH-H)
UART0	<b>[Disabled]</b> [Enabled]	Checked = Pin set to ISH Native function. Checkbox grayed out = disable conflicting SerialIo controller to set. Shared pins: 1. ISH UART0 - LPSS I2C2(PCH-H) 2. ISH UART1 - LPSS UART1 3. ISH I2C2 - LPSS I2C5(PCH-LP) / I2C3(PCH-H)
UART1	<b>[Disabled]</b> [Enabled]	Checked = Pin set to ISH Native function.

		<p>Checkbox grayed out = disable conflicting SerialIo controller to set.</p> <p>Shared pins:</p> <ol style="list-style-type: none"> <li>1. ISH UART0 - LPSS I2C2(PCH-H)</li> <li>2. ISH UART1 - LPSS UART1</li> <li>3. ISH I2C2 - LPSS I2C5(PCH-LP) / I2C3(PCH-H)</li> </ol>
I2C0	[Disabled] <b>[Enabled]</b>	<p>Checked = Pin set to ISH Native function.</p> <p>Checkbox grayed out = disable conflicting SerialIo controller to set.</p> <p>Shared pins:</p> <ol style="list-style-type: none"> <li>1. ISH UART0 - LPSS I2C2(PCH-H)</li> <li>2. ISH UART1 - LPSS UART1</li> <li>3. ISH I2C2 - LPSS I2C5(PCH-LP) / I2C3(PCH-H)</li> </ol>
I2C1	[Disabled] <b>[Enabled]</b>	<p>Checked = Pin set to ISH Native function.</p> <p>Checkbox grayed out = disable conflicting SerialIo controller to set.</p> <p>Shared pins:</p> <ol style="list-style-type: none"> <li>1. ISH UART0 - LPSS I2C2(PCH-H)</li> <li>2. ISH UART1 - LPSS UART1</li> <li>3. ISH I2C2 - LPSS I2C5(PCH-LP) / I2C3(PCH-H)</li> </ol>
I2C2	<b>[Disabled]</b> [Enabled]	<p>Checked = Pin set to ISH Native function.</p> <p>Checkbox grayed out = disable conflicting SerialIo controller to set.</p> <p>Shared pins:</p> <ol style="list-style-type: none"> <li>1. ISH UART0 - LPSS I2C2(PCH-H)</li> <li>2. ISH UART1 - LPSS UART1</li> <li>3. ISH I2C2 - LPSS I2C5(PCH-LP) / I2C3(PCH-H)</li> </ol> <p><u>(This option can be set at I2C5 Controller set Disabled)</u></p>
GP_0	[Disabled] <b>[Enabled]</b>	<p>Checked = Pin set to ISH Native function.</p> <p>Checkbox grayed out = disable conflicting SerialIo controller to set.</p> <p>Shared pins:</p> <ol style="list-style-type: none"> <li>1. ISH UART0 - LPSS I2C2(PCH-H)</li> <li>2. ISH UART1 - LPSS UART1</li> <li>3. ISH I2C2 - LPSS I2C5(PCH-LP) / I2C3(PCH-H)</li> </ol>
GP_1	[Disabled] <b>[Enabled]</b>	<p>Checked = Pin set to ISH Native function.</p>

		<p>Checkbox grayed out = disable conflicting SerialIo controller to set.</p> <p>Shared pins:</p> <ol style="list-style-type: none"> <li>1. ISH UART0 - LPSS I2C2(PCH-H)</li> <li>2. ISH UART1 - LPSS UART1</li> <li>3. ISH I2C2 - LPSS I2C5(PCH-LP) / I2C3(PCH-H)</li> </ol>
GP_2	[Disabled] <b>[Enabled]</b>	<p>Checked = Pin set to ISH Native function.</p> <p>Checkbox grayed out = disable conflicting SerialIo controller to set.</p> <p>Shared pins:</p> <ol style="list-style-type: none"> <li>1. ISH UART0 - LPSS I2C2(PCH-H)</li> <li>2. ISH UART1 - LPSS UART1</li> <li>3. ISH I2C2 - LPSS I2C5(PCH-LP) / I2C3(PCH-H)</li> </ol>
GP_3	[Disabled] <b>[Enabled]</b>	<p>Checked = Pin set to ISH Native function.</p> <p>Checkbox grayed out = disable conflicting SerialIo controller to set.</p> <p>Shared pins:</p> <ol style="list-style-type: none"> <li>1. ISH UART0 - LPSS I2C2(PCH-H)</li> <li>2. ISH UART1 - LPSS UART1</li> <li>3. ISH I2C2 - LPSS I2C5(PCH-LP) / I2C3(PCH-H)</li> </ol>
GP_4	[Disabled] <b>[Enabled]</b>	<p>Checked = Pin set to ISH Native function.</p> <p>Checkbox grayed out = disable conflicting SerialIo controller to set.</p> <p>Shared pins:</p> <ol style="list-style-type: none"> <li>1. ISH UART0 - LPSS I2C2(PCH-H)</li> <li>2. ISH UART1 - LPSS UART1</li> <li>3. ISH I2C2 - LPSS I2C5(PCH-LP) / I2C3(PCH-H)</li> </ol>
GP_5	[Disabled] <b>[Enabled]</b>	<p>Checked = Pin set to ISH Native function.</p> <p>Checkbox grayed out = disable conflicting SerialIo controller to set.</p> <p>Shared pins:</p> <ol style="list-style-type: none"> <li>1. ISH UART0 - LPSS I2C2(PCH-H)</li> <li>2. ISH UART1 - LPSS UART1</li> <li>3. ISH I2C2 - LPSS I2C5(PCH-LP) / I2C3(PCH-H)</li> </ol>
GP_6	[Disabled] <b>[Enabled]</b>	<p>Checked = Pin set to ISH Native function.</p> <p>Checkbox grayed out = disable conflicting SerialIo controller to set.</p>

		Shared pins: 1. ISH UART0 - LPSS I2C2(PCH-H) 2. ISH UART1 - LPSS UART1 3. ISH I2C2 - LPSS I2C5(PCH-LP) / I2C3(PCH-H)
GP_7	[Disabled] <b>[Enabled]</b>	Checked = Pin set to ISH Native function. Checkbox grayed out = disable conflicting SerialIo controller to set. Shared pins: 1. ISH UART0 - LPSS I2C2(PCH-H) 2. ISH UART1 - LPSS UART1 3. ISH I2C2 - LPSS I2C5(PCH-LP) / I2C3(PCH-H)

### 2.2.17.10 Pch Thermal Throttling Control

**Table 2-2-17-10. Pch Thermal Throttling Control**

BIOS Setting	Options	Description
Thermal Throttling Level	<b>[Suggested Setting]</b> [Manual]	Determine if use Intel suggested setting (Below options will show at this option set Manual.)
Thermal Throttling	<b>[Disabled]</b> [Enabled]	Enable/Disable the thermal throttling states control
TT State 13	<b>[Disabled]</b> [Enabled]	PMSync state 13 will force at least T2 state
Thermal Throttling Lock	<b>[Disabled]</b> [Enabled]	Lock the entire TL register
T0 Level	<b>minimum = 0</b> <b>maximum = 65535</b> <b>step = 1</b> <b>default = 0</b>	If Trip Point Temperature <= T0Level, the system is in T0 state
T1 Level	<b>minimum = 0</b> <b>maximum = 65535</b> <b>step = 1</b> <b>default = 0</b>	If T1Level >= Trip Point Temperature > T0Level, the system is in T1 state
T2 Level	<b>minimum = 0</b> <b>maximum = 65535</b> <b>step = 1</b> <b>default = 0</b>	If T2Level >= Trip Point Temperature > T1Level, the system is in T2 state
DMI Thermal Setting	<b>[Suggested Setting]</b> [Manual]	Determine if use Intel suggested setting (Below options will show at this option set Manual.)
DMI Thermal Sensor Autonomous Width	<b>[Disabled]</b> [Enabled]	Enable/Disable Thermal Sensor initiated Autonomous Width Negotiation

Thermal Sensor 0 Width	[x1] [x2] [x4] <b>[x8]</b> [x16]	Determine the DMI Link Width when the output from the Thermal Sensor is T0
Thermal Sensor 1 Width	[x1] [x2] <b>[x4]</b> [x8] [x16]	Determine the DMI Link Width when the output from the Thermal Sensor is T1
Thermal Sensor 2 Width	[x1] <b>[x2]</b> [x4] [x8] [x16]	Determine the DMI Link Width when the output from the Thermal Sensor is T2
Thermal Sensor 3 Width	<b>[x1]</b> [x2] [x4] [x8] [x16]	Determine the DMI Link Width when the output from the Thermal Sensor is T3
SATA Thermal Setting	<b>[Suggested Setting]</b> [Manual]	Determine if use Intel suggested setting (Below options will show at this option set Manual.)
Port 0		
T1 Multiplier	[Disabled] <b>[x1]</b> [x2] [x4]	Determine the value of SATA Port T1 Multiplier
T2 Multiplier	[Disabled] [x1] <b>[x2]</b> [x4]	Determine the value of SATA Port T2 Multiplier
T3 Multiplier	[Disabled] [x1] [x2] <b>[x4]</b>	Determine the value of SATA Port T3 Multiplier
Alternate Fast Init Tdispatch	<b>[Disabled]</b> [Enabled]	Enable/Disable SATA Port Alternate Fast Init Tdispatch
(Below option will show at Alternate Fast Init Tdispatch set Enabled)		
Tdispatch	<b>[~32us]</b> [~128us] [~8us]	Determine the value of SATA Port Tdispatch
Tinactive	<b>[~32us]</b> [~128us] [~8us]	Determine the value of SATA Port Tinactive
(Below option will show at Alternate Fast Init Tdispatch set Disabled)		
Tdispatch	<b>[~32ms]</b> [~128ms] [~8ms]	Determine the value of SATA Port Tdispatch
Tinactive	<b>[~32ms]</b> [~128ms] [~8ms]	Determine the value of SATA Port Tinactive
Port 1		
T1 Multiplier	[Disabled] <b>[x1]</b> [x2] [x4]	Determine the value of SATA Port T1 Multiplier
T2 Multiplier	[Disabled] [x1] <b>[x2]</b> [x4]	Determine the value of SATA Port T2 Multiplier
T3 Multiplier	[Disabled] [x1] [x2] <b>[x4]</b>	Determine the value of SATA Port T3 Multiplier

Alternate Fast Init Tdispatch	<b>[Disabled]</b> [Enabled]	Enable/Disable SATA Port Alternate Fast Init Tdispatch
<u>(Below option will show at Alternate Fast Init Tdispatch set Enabled)</u>		
Tdispatch	<b>[~32us]</b> [~128us] [~8us]	Determine the value of SATA Port Tdispatch
Tinactive	<b>[~32us]</b> [~128us] [~8us]	Determine the value of SATA Port Tinactive
<u>(Below option will show at Alternate Fast Init Tdispatch set Disabled)</u>		
Tdispatch	<b>[~32ms]</b> [~128ums] [~8ms]	Determine the value of SATA Port Tdispatch
Tinactive	<b>[~32ms]</b> [~128ms] [~8ms]	Determine the value of SATA Port Tinactive

### 2.2.17.11 FIVR Configuration

**Table 2-2-17-11. FIVR Configuration**

BIOS Setting	Options	Description
External V1P05 Rail Sx/S0ix Configuration		External V1P05 Rail Sx/S0ix Configuration
Enable Rail in S0i1/S0i2	<b>[Disabled]</b> [Enabled]	Enable/Disable the thermal throttling states control
Enable Rail in S0i3	<b>[Disabled]</b> [Enabled]	Enables External V1P05 Rail in corresponding Sx/S0ix
Enable Rail in S3	<b>[Disabled]</b> [Enabled]	Enables External V1P05 Rail in corresponding Sx/S0ix
Enable Rail in S4	<b>[Disabled]</b> [Enabled]	Enables External V1P05 Rail in corresponding Sx/S0ix
Enable Rail in S5	<b>[Disabled]</b> [Enabled]	Enables External V1P05 Rail in corresponding Sx/S0ix
Enable Rail in S0	<b>[Disabled]</b> [Enabled]	Enables External V1P05 Rail in corresponding Sx/S0ix
External Vnn Rail Sx/S0ix Configuration		External Vnn Rail Sx/S0ix Configuration
Enable Rail in S0i1/S0i2	<b>[Disabled]</b> [Enabled]	Enable/Disable the thermal throttling states control
Enable Rail in S0i3	<b>[Disabled]</b> [Enabled]	Enables External Vnn Rail in corresponding Sx/S0ix
Enable Rail in S3	<b>[Disabled]</b> [Enabled]	Enables External Vnn Rail in corresponding Sx/S0ix
Enable Rail in S4	<b>[Disabled]</b> [Enabled]	Enables External Vnn Rail in corresponding Sx/S0ix
Enable Rail in S5	<b>[Disabled]</b> [Enabled]	Enables External Vnn Rail in corresponding Sx/S0ix

Enable Rail in S0	<b>[Disabled]</b> [Enabled]	Enables External Vnn Rail in corresponding Sx/S0ix
External Vnn Rail Voltage Configuration	[0.7V@Bypass - 0.75V@Internal - 1.05V@Internal] [0.75V@Bypass - 0.75V@Bypass - 1.05V@Internal] [0.7V@Bypass - 0.75V@Bypass - 1.05V@Internal] <b>[1.05V@Bypass - 1.05V@Bypass - 1.05V@Bypass]</b>	Configures TARGET_VOLT_LEVEL for External Rail
External Rails Voltage and Current settings		External Rails Voltage and Current settings
External V1P05 Icc Max Valu	<b>minimum = 0</b> <b>maximum = 500</b> <b>step = 1</b> <b>default = 500</b>	Icc Max Value for external V1p05 rail. Expressed in mA. Accepted value are between 0 and 500 mA
External Vnn Icc Max Value	<b>minimum = 0</b> <b>maximum = 500</b> <b>step = 1</b> <b>default = 500</b>	Icc Max Value for external Vnn rail. Expressed in mA. Accepted value are between 0 and 500 mA
VCCIN_AUX voltage rail timing configuration		VCCIN_AUX voltage rail timing configuration
Retention to Low Current Mode	<b>minimum = 0</b> <b>maximum = 255</b> <b>step = 1</b> <b>default = 0</b>	Transition time in microseconds from Off (0V) to High Current Mode Voltage. This field has 1us resolution.
Retention to High Current Mode	<b>minimum = 0</b> <b>maximum = 255</b> <b>step = 1</b> <b>default = 0</b>	Transition time in microseconds from Retention Mode Voltage to High Current Mode Voltage. This field has 1us resolution.
Low to High Current Mode	<b>minimum = 0</b> <b>maximum = 255</b> <b>step = 1</b> <b>default = 0xC</b>	Transition time in microseconds from Low Current Mode Voltage to High Current Mode Voltage. This field has 1us resolution.
Off to High Current Mode	<b>minimum = 0</b> <b>maximum = 255</b> <b>step = 1</b> <b>default = 96</b>	Transition time in microseconds from Off (0V) to High Current Mode Voltage. This field has 1us resolution. 0 = Transition to 0V is disabled
FIVR Dynamic PM	[Disabled] <b>[Enabled]</b>	Enable/Disable FIVR Dynamic Power Management

## 2.2.17.12 PMC Configuration

**Table 2-2-17-12. PMC Configuration**

BIOS Setting	Options	Description
PMC Configuration		
PMC ADR Configuration	(See Section 2.2.17.12.1)	PMC ADR Configuration

### 2.2.17.12.1 PMC ADR Configuration

**Table 2-2-17-12-1. PMC ADR Configuration**

BIOS Setting	Options	Description
PMC ADR Configuration		
ADR enable	<b>[Platform-POR]</b> [Enable] [Disabled]	Enable asynchronous DRAM refresh <i>(Below will show at this not set Disabled)</i>
Host Partition Reset ADR Enable	<b>[Platform-POR]</b> [Enable] [Disabled]	Enables/Disables ADR on Host Partition Reset
ADR timer 1 expire time	<b>minimum = 0</b> <b>maximum = 0xFF</b> <b>step = 1</b> <b>default = 32</b>	Type desired ADR timer expire time, valid values - <1, 256>. Entered time is scaled by ADR timer time unit.
ADR timer 1 time unit	[1us] [10us] [100us] [1ms] [10ms] [100ms] <b>[1s]</b> [10s]	Select ADR timer time unit.

## 2.2.18 PCH-FW Configuration

**Table 2-2-18. PCH-FW Configuration**

BIOS Setting	Options	Description
ME Firmware Version	No options	ME Firmware Version
ME Firmware Mode	No options	ME Firmware Mode
ME Firmware SKU	No options	ME Firmware SKU
ME Firmware Status 1	No options	ME Firmware Status 1
ME Firmware Status 2	No options	ME Firmware Status 2
ME State	[Disabled] <b>[Enabled]</b>	When Disabled ME will be put into ME Temporarily Disabled Mode. (Show as <u>ME_SETUP_STORAGE.RemoteSessionActive</u> is not 0x1 OR <u>ME_SETUP_STORAGE.AfterEoP</u> is not 0x1)

Manageability Features State	[Disabled] <b>[Enabled]</b>	Enable/Disable Intel(R) Manageability features. NOTE: This option disables/enables Manageability Features support in FW. To disable support platform must be in an unprovisioned state first. (Show as <u>AMT_SUPPORT</u> is true)
AMT BIOS Features	[Disabled] <b>[Enabled]</b>	When disabled AMT BIOS Features are no longer supported and user is no longer able to access MEBx Setup. Note: This option does not disable Manageability Features in FW. (Show as <u>AMT_SUPPORT</u> is true)
AMT Configuration	(See Section 2.2.18.1)	Configure Intel(R) Active Management Technology Parameters (Show as <u>AMT_SUPPORT</u> is true)
ME Unconfig on RTC Clear	[Disabled] <b>[Enabled]</b>	When Disabled ME will be unconfigured on RTC Clear.
Comms Hub Support	<b>[Disabled]</b> [Enabled]	Enable/Disable support for Comms Hub.
JHI Support	<b>[Disabled]</b> [Enabled]	Enable/Disable Intel(R) DAL Host Interface Service(JHI)
Core Bios Done Message	[Disabled] <b>[Enabled]</b>	Enable/Disable Core Bios Done Message sent to ME
Firmware Update Configuration	(See Section 2.2.18.2)	Configure Management Engine Technology Parameters
PTT Configuration	(See Section 2.2.18.3)	Configuration PTT
FIPS Configuration	(See Section 2.2.18.4)	FIPS Mode help
ME Debug Configuration	(See Section 2.2.18.5)	Configuration ME debug options NOTE: This menu is provided for testing purposes. It is recommended to leave the options in their default states.
Anti-Rollback SVN Configuration	(See Section 2.2.18.6)	Configure Anti-Rollback SVN
Extend CSME Measurement to TPM-PCR	<b>[Disabled]</b> [Enabled]	Enable/Disable Extend CSME Measurement to TPM-PCR[0] and AMT Config to TPM-PCR[1]

### 2.2.18.1 AMT Configuration

**Table 2-2-18-1. AMT Configuration**

BIOS Setting	Options	Description
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USB Provisioning of AMT	<b>[Disabled]</b> [Enabled]	Enable/Disable of AMT USB Provisioning.
CIRA Configuration	(See Section 2.2.18.1.1)	Configure Remote Assistance Process parameters.
ASF Configuration	(See Section 2.2.18.1.2)	Configure Alert Standard Format parameters.
Secure Erase Configuration	(See Section 2.2.18.1.3)	Secure Erase configuration menu
OEM Flags Settings	(See Section 2.2.18.1.4)	Configure OEM Flags
MEBx Resolution Settings	(See Section 2.2.18.1.5)	Resolution settings for MEBx display modes

### 2.2.18.1.1 CIRA Configuration

**Table 2-2-18-1-1. CIRA Configuration**

BIOS Setting	Options	Description
Activate Remote Assistance Process	<b>[Disabled]</b> [Enabled]	Trigger CIRA boot Note: Network Access must be activated first from MEBx Setup.
CIRA Timeout	<b>minimum = 0 maximum = 255 step = 1 default = 0</b>	OEM defined timeout for MPS connection to be established. 0 - use the default timeout value of 60 seconds. 255 - MEBx waits until the connection succeeds

### 2.2.18.1.2 ASF Configuration

**Table 2-2-18-1-2. ASF Configuration**

BIOS Setting	Options	Description
PET Progress	[Disabled] <b>[Enabled]</b>	Enable/Disable PET Events Progress to receive PET Events.
WatchDog	<b>[Disabled]</b> [Enabled]	Enable/Disable WatchDog Timer.
OS Timer	<b>minimum = 0 maximum = 65535 step = 1 default = 0</b>	Set OS watchdog timer.
BIOS Timer	<b>minimum = 0 maximum = 65535 step = 1 default = 0</b>	Set BIOS watchdog timer.
ASF Sensors Table	<b>[Disabled]</b> [Enabled]	Adds ASF Sensor Table into ASF! ACPI Table

### 2.2.18.1.3 Secure Erase Configuration

**Table 2-2-18-1-3. Secure Erase Configuration**

BIOS Setting	Options	Description
Secure Erase mode	<b>[Simulated]</b> [Real]	Change Secure Erase module behavior: Simulated: Performs SE flow without erasing SSD Real: Erase SSD.
Force Secure Erase	<b>[Disabled]</b> [Enabled]	Force Secure Erase on next boot

### 2.2.18.1.4 OEM Flags Settings

**Table 2-2-18-1-4. OEM Flags Settings**

BIOS Setting	Options	Description
MEBx hotkey Pressed	<b>[Disabled]</b> [Enabled]	OEMFlag Bit 1: Enable automatic MEBx hotkey press.
MEBx Selection Screen	<b>[Disabled]</b> [Enabled]	OEMFlag Bit 2: Enable MEBx selection screen with 2 options: Press 1 to enter ME Configuration Screens Press 2 to initiate a remote connection Note: Network Access must be activated from MEBx Setup for this screen to be displayed.
Hide Unconfigure ME Confirmation Prompt	<b>[Disabled]</b> [Enabled]	OEMFlag Bit 6: Hide Unconfigure ME confirmation prompt when attempting ME unconfiguration.
MEBx OEM Debug Menu Enable	<b>[Disabled]</b> [Enabled]	OEMFlag Bit 14: Enable OEM debug menu in MEBx.
Unconfigure ME	<b>[Disabled]</b> [Enabled]	OEMFlag Bit 15: Unconfigure ME with resetting MEBx password to default.

### 2.2.18.1.5 MEBx Resolution Settings

**Table 2-2-18-1-5. MEBx Resolution Settings**

BIOS Setting	Options	Description
Non-UI Mode Resolution	[Auto] [80x25] [100x31]	Resolution for non-UI text mode.
UI Mode Resolution	<b>[Auto]</b> [80x25] [100x31]	Resolution for UI text mode.

Graphics Mode Resolution	<b>[Auto]</b> [640x480] [800x600] [1024x768]	Resolution for graphics mode.
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### 2.2.18.2 Firmware Update Configuration

**Table 2-2-18-2. Firmware Update Configuration**

BIOS Setting	Options	Description
ME FW Image Re-Flash	<b>[Disabled]</b> [Enabled]	Enable/Disable ME FW Image Re-Flash function.
FW Update	[Disabled] <b>[Enabled]</b>	Enable/Disable ME FW Update function. (Show as <u>ME_SETUP_STORAGE.AfterEoP</u> is not 0x1)

### 2.2.18.3 PTT Configuration

**Table 2-2-18-3. PTT Configuration**

BIOS Setting	Options	Description
PTT Capability / State	No options	Platform Trust Technology Capability / Enablement State.
TPM 1.2 Deactivate	<b>[Disabled]</b> [Enabled]	Enabling this option will invoke the TPM 1.2 De-activate flow. (Show as <u>ME_SETUP_STORAGE.AfterEoP</u> is not 0x1 <u>ME_SETUP_STORAGE.BootGuardSupport</u> is not 0 OR <u>SystemConfig.TpmDeviceOk</u> is 1 OR <u>ME_SETUP_STORAGE.MeasureBoot</u> is not 0)

### 2.2.18.4 FIPS Mode

**Table 2-2-18-4. FIPS Mode**

BIOS Setting	Options	Description
FIPS Mode Select	<b>[Disabled]</b> [Enabled]	FIPS Mode configuration. ( <u>Below will show at this set to Enable</u> )
FIPS Mode auto sync	<b>[Disabled]</b> [Enabled]	When enabled, it always synchronizes FIPS mode automatically. (Spending 250ms at least)
Current FIPS mode	No options	N/A

Crypto driver FIPS version	No options	N/A
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### 2.2.18.5 ME Debug Configuration

**Table 2-2-18-5. ME Debug Configuration**

BIOS Setting	Options	Description
HECI Timeouts	[Disabled] <b>[Enabled]</b>	Enable/Disable HECI Send/Receive Timeouts.
Force ME DID Init Status	<b>[Disabled]</b> [0 - Success] [1 - No Memory in Channels] [2 - Memory Init Error]	Forces the DID Initialization Status value.
CPU Replaced Polling Disable	<b>[Disabled]</b> [Enabled]	Setting this options disables CPU replacement polling loop.
HECI Message check Disable	<b>[Disabled]</b> [Enabled]	Setting this option disables message check for Bios Boot Path when sending.
MBP HOB Skip	<b>[Disabled]</b> [Enabled]	Setting this option will skip MBP HOB.
HECI2 Interface Communication	<b>[Disabled]</b> [Enabled]	Adds and Removes HECI2 Device from PCI space.
KT Device	[Disabled] <b>[Enabled]</b>	Enable/Disable KT Device.
End of Post Message	[Disabled] <b>[Send in DXE]</b>	Enable/Disable End of Post Message sent to ME.
D0I3 Setting for HECI Disable	<b>[Disabled]</b> [Enabled]	Setting this option disables setting D0I3 bit for all HECI devices.
MCTP Broadcast Cycle	<b>[Disabled]</b> [Enabled]	Enable/Disable Management Component Transport Protocol Broadcast Cycle and Set PMT as Bus Owner.

### 2.2.18.6 Anti-Rollback SVN Configuration

**Table 2-2-18-6. Anti-Rollback SVN Configuration**

BIOS Setting	Options	Description
Minimal Allowed Anti-Rollback SVN	No options	Minimum ARB-SVN allowed on this platform. ME FW with lower ARB-SVN will not boot.
Executing Anti-Rollback SVN	No options	ARB-SVN of executing ME FW.
Below option will grayout if (Show as <i>ME_SETUP_STORAGE.AfterEoP</i> is not 0x1)		

Automatic HW-Enforced Anti-Rollback SVN	<b>[Disabled]</b> [Enabled]	When enabled, hardware-enforced Anti-Rollback mechanism is automatically activated: once ME FW was successfully run on a platform, FW with lower ARB-SVN will be blocked from execution.
Set HW-Enforced Anti-Rollback for Current SVN	<b>[Disabled]</b> [Enabled]	Enable hardware-enforced Anti-Rollback mechanism for current ARB-SVN value. FW with lower ARB-SVN will be blocked from execution. The value will be restored to disable after the command is sent. (Show as <u>ME_SETUP.AutoArbSvnCommit</u> is not 1)

## 2.2.19 Thermal Configuration

**Table 2-2-19. Thermal Configuration**

BIOS Setting	Options	Description
Thermal Configuration		
Enable All Thermal Functions	[Disabled] <b>[Enabled]</b>	Enable All Thermal Functions" is Enabled it Enables 'Memory Thermal Management', 'Active Trip Points', 'Critical Trip Points'.Set to disabled for Manual Configuration
CPU Thermal Configuration	(See Section 2.2.19.1)	CPU Thermal Configuration options.
Platform Thermal Configuration	(See Section 2.2.19.2)	Platform Thermal Configuration options.
Intel(R) Dynamic Tuning Configuration	(See Section 2.2.19.3)	Intel(R) Dynamic Tuning Configuartions options.
Hardware Health Monitor	(See Section 2.2.19.4)	Monitor the Hardware Health.

### 2.2.19.1 CPU Thermal Configuration

**Table 2-2-19-1. CPU Thermal Configuration**

BIOS Setting	Options	Description
Cpu Thermal Configuration		
Tcc Activation offset	<b>minimum = 0</b> <b>maximum = 0x3F</b> <b>step = 0</b> <b>default = 0</b>	Offset from factory set Tcc activation temperature at which the Thermal Control Circuit must be activated.

		Tcc will be activated at: Tcc Activation Temp - Tcc Activation Offset. Tcc Activation Offset range is 0 to 63.
Tcc Offset Time Window	<b>[Disabled]</b> [5ms][10ms] [55ms] [156ms][375ms][500ms][750ms] [1sec][2sec] [3sec][4sec] [5sec][6sec][7sec][8sec] [10sec][12sec][14sec][16sec] [20sec][24sec] [28sec][32sec] [40sec][48sec] [56sec][64sec][80sec][96sec] [112sec][128sec][160sec][192sec] [224sec][256sec][320sec][384sec][448sec]	Tcc Offset Time Window for Running Average Temperature Limit(RATL) feature. The Tcc offset time window can range from 5ms to 448s.
Tcc Offset Clamp Enable	<b>[Disabled]</b> [Enabled]	Tcc Offset Clamp bit Enable for Running Average Temperature Limit(RATL) feature to allow CPU to throttle below P1.
Tcc Offset Lock Enable	[Disabled] <b>[Enabled]</b>	Lock Enable for Running Average Temperature Limit(RATL) feature to lock Temperature Target MSR.
Bi-directional PROCHOT#	[Disabled] <b>[Enabled]</b>	When a processor thermal sensor trips (either core), the PROCHOT# will be driven. If bi-direction is enabled, external agents can drive PROCHOT# to throttle the processor.
Disable PROCHOT# Output	[Disabled] <b>[Enabled]</b>	Enable/Disable PROCHOT# Output. (Show as <u>CPU_SETUP.EnableProHot</u> is not 0x0)
Disable VR Thermal Alert	<b>[Disabled]</b> [Enabled]	Enable/Disable VR Thermal Alert.
PROCHOT Response	[Disabled] <b>[Enabled]</b>	Enable/Disable PROCHOT Response.
PROCHOT Lock	[Disabled] <b>[Enabled]</b>	Enable/Disable PROCHOT Lock.
ACPI T-States	<b>[Disabled]</b> [Enabled]	Enable/Disable ACPI T-States.

## 2.2.19.2 Platform Thermal Configuration

**Table 2-2-19-2. Platform Thermal Configuration**

BIOS Setting	Options	Description
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Platform Thermal Configuration		
Critical Trip Point	[15C] [23C] [31C] [39C] [47C][55C] [63C] [71C] [79C] [87C][95C] [100C] [103C] [111C] <b>[119C(POR)]</b> [127C]	This value controls the temperature of the ACPI Critical Trip Point - the point in which the OS will shut the system off. Note: 119C is the Plan of Record (POR) for all Intel mobile processors. (Show as <u>CPU_SETUP.AutoThermalReporting</u> is not 1)
Active Trip Point 0	[Disabled] [15C] [23C] [31C] [39C] [47C] [55C] [63C] <b>[71C]</b> [79C] [87C] [95C] [103C] [111C] [119C(POR)]	This value controls the temperature of the ACPI Active Trip Point 0 - the point in which the OS will turn the processor fan on Active Trip Point 0 Fan Speed. (Show as <u>CPU_SETUP.AutoThermalReporting</u> is not 1)
Active Trip Point 0 Fan Speed	<b>minimum = 0</b> <b>maximum = 100</b> <b>step = 1</b> <b>default = 100</b>	Active Trip Point 0 Fan Speed in percentage. Value must be between 0 (Fan off) - 100 (Max fan speed). This is the speed at which fan will run when Active Trip Point 0 is crossed.
Active Trip Point 1	[Disabled] [15C] [23C] [31C] [39C] [47C] <b>[55C]</b> [63C] [71C][79C] [87C] [95C] [103C] [111C] [119C(POR)]	This value controls the temperature of the ACPI Active Trip Point 1 - the point in which the OS will turn the processor fan on Active Trip Point 1 Fan Speed.
Active Trip Point 1 Fan Speed	<b>minimum = 0</b> <b>maximum = 100</b> <b>step = 1</b> <b>default = 75</b>	Active Trip Point 1 Fan Speed in percentage. Value must be between 0 (Fan off) - 100 (Max fan speed). This value must be less than Active Trip Point 0 Fan speed. This is the speed at which fan will run when Active Trip 1 is crossed.
Passive Trip Point	[Disabled] [15C] [23C] [31C] [39C] [47C] [55C] [63C] [71C] [79C] [87C] <b>[95C]</b> [103C] [111C] [119C(POR)]	This value controls the temperature of the ACPI Passive Trip Point - the point in which the OS will begin throttling the processor. (Show as <u>CPU_SETUP.AutoThermalReporting</u> is not 1)
Passive TC1 Value	<b>minimum = 1</b> <b>maximum = 16</b> <b>step = 1</b> <b>default = 1</b>	This value sets the TC1 value for the ACPI Passive Cooling Formula. Range 1 - 16

Passive TC2 Value	<b>minimum = 1</b> <b>maximum = 16</b> <b>step = 1</b> <b>default = 5</b>	This value sets the TC2 value for the ACPI Passive Cooling Formula. Range 1 - 16
Passive TSP Value	<b>minimum = 2</b> <b>maximum = 32</b> <b>step = 2</b> <b>default = 10</b>	This item sets the TSP value for the ACPI Passive Cooling Formula. It represents in tenths of a second how often the OS will read the temperature when passive cooling is enabled. Range 2 - 32
Active Trip Points	[Disabled] <b>[Enabled]</b>	Disable Active Trip Points.
Passive Trip Points	<b>[Disabled]</b> [Enabled]	Disable Passive Trip Points.
Critical Trip Points	[Disabled] <b>[Enabled]</b>	Disable Critical Trip Points.
PCH Temp Read	[Disabled] <b>[Enabled]</b>	PCH Temperature Read Enable.
CPU Energy Read	[Disabled] <b>[Enabled]</b>	CPU Energy Read Enable
CPU Temp Read	[Disabled] <b>[Enabled]</b>	CPU Temperature Read Enable
Alert Enable Lock	<b>[Disabled]</b> [Enabled]	Lock all Alert Enable settings. (Below options will show at this options enabled.)
PCH Alert	<b>[Disabled]</b> [Enabled]	PCH Alert pin enable.
DIMM Alert	<b>[Disabled]</b> [Enabled]	DIMM Alert pin enable.
CPU Temp	<b>minimum = 1</b> <b>maximum = 110</b> <b>step = 1</b> <b>default = 72</b>	Fail Safe temp that EC will use if OS is hung.
CPU Fan Speed	<b>minimum = 1</b> <b>maximum = 100</b> <b>step = 1</b> <b>default = 65</b>	Fan speed that EC will use if OS is hung.

### 2.2.19.3 Intel(R) Dynamic Tuning Configuration

**Table 2-2-19-3. Intel(R) Dynamic Tuning Configuration**

BIOS Setting	Options	Description
Intel(R) Dynamic Tuning Configuration		
Intel(R) Dynamic Tuning	[Disabled] <b>[Enabled]</b>	Enable/Disable Intel(R) Dynamic Tuning
<u>(Below options will show at Intel(R) Dynamic Tuning set enabled.)</u>		

Processor Thermal Device	[Disabled] <b>[SA Thermal Device]</b>	Enable/Disable Processor Thermal Device.
<u>(Below options will show at this option set SA Thermal Device.)</u>		
Active Thermal Trip Point	<b>minimum = 0</b> <b>maximum = 127</b> <b>step = 1</b> <b>default = 90</b>	This value controls the temperature of the ACPI Active Thermal Trip Point. NOTE: a value of zero will cause the Intel Dynamic Tuning driver to disable the trip point.
Passive Thermal Trip Point	<b>minimum = 0</b> <b>maximum = 127</b> <b>step = 1</b> <b>default = 110</b>	This value controls the temperature of the ACPI Passive Thermal Trip Point. NOTE: a value of zero will cause the Intel Dynamic Tuning driver to disable the trip point.
Critical Thermal Trip Point	<b>minimum = 0</b> <b>maximum = 127</b> <b>step = 1</b> <b>default = 110</b>	This value controls the temperature of the ACPI Critical Thermal Trip Point. NOTE: a value of zero will cause the Intel Dynamic Tuning driver to disable the trip point.
S3/CS Thermal Trip Point	<b>minimum = 0</b> <b>maximum = 127</b> <b>step = 1</b> <b>default = 110</b>	This value controls the temperature of the ACPI Critical Thermal Trip Point for entering S3 or CS. NOTE: a value of zero will cause the Intel Dynamic Tuning driver to disable the trip point.
Hot Thermal Trip Point	<b>minimum = 0</b> <b>maximum = 127</b> <b>step = 1</b> <b>default = 110</b>	This value controls the temperature of the ACPI Hot Thermal Trip Point. NOTE: a value of zero will cause the Intel Dynamic Tuning driver to disable the trip point.
Thermal Sampling Period	<b>minimum = 0</b> <b>maximum = 100</b> <b>step = 1</b> <b>default = 0</b>	The polling interval in 10ths of seconds. A value of 0 tells the driver to use interrupts. NOTE: The granularity of the sampling period is 0.1 seconds. For example, if the sampling period is 30 seconds, then _TSP needs to report 300; if the sampling period is 0.5 seconds, then choose 5.
PPCC Step Size	<b>[0.5 Watts]</b> [1.0 Watts] [1.5 Watts] [2.0 Watts]	Step size for Turbo power limit (RAPL) control.
Maximum Power Limit 1	No options	Power Limit 1 in Milli Watts. BIOS will round to the nearest 1/8W when programming. 0 = no custom override. For 12.50W, enter 12500. Overclocking SKU: Value must be between Max and Min Power Limits (specified by PACKAGE_POWER_SKU_MSR). Other SKUs: This value must be between Min Power Limit and TDP Limit. If value is 0, BIOS will program TDP value.
Minimum Power Limit (cTDP Nom)	<b>minimum = 0</b> <b>maximum = 30000</b> <b>step = 125</b>	This value provides the minimum power limit in the PPCC object for this platform at

	<b>default = 125</b>	cTDP Level 0 (Nominal). Enter the value in milliwatts with 125mw granularity.
Minimum Power Limit (cTDP Down)	<b>minimum = 0</b> <b>maximum = 30000</b> <b>step = 125</b> <b>default = 125</b>	This value provides the minimum power limit in the PPCC object for this platform cTDP Level 1 (Down). Enter the value in milliwatts with 125mw granularity.
Minimum Power Limit (cTDP up)	<b>minimum = 0</b> <b>maximum = 30000</b> <b>step = 125</b> <b>default = 125</b>	This value provides the minimum power limit in the PPCC object for this platform cTDP Level 2 (Up). Enter the value in milliwatts with 125mw granularity.
CLPO Enable	[Disabled] <b>[Enabled]</b>	Instructs the policy to use Active Cores if they are available.
CLPO Start PState	<b>minimum = 0</b> <b>maximum = 16</b> <b>step = 1</b> <b>default = 16</b>	Instructs the policy when to initiate Active Core control if enabled. Note: 16=LFM
CLPO Step Size	<b>minimum = 0</b> <b>maximum = 100</b> <b>step = 1</b> <b>default = 50</b>	Instructs the policy to take away logical processors in the specified percentage steps.
CLPO Power Control	[Disabled] <b>[SMT off lining]</b> [Core Off lining]	Instructs the policy whether to use Core offlining or SMT offlining if Active core control is enabled to be used in P0 or when power control is applied.
CLPO Performance Control	[Disabled] [SMT off lining] <b>[Core Off lining]</b>	Instructs the policy whether to use Core offlining or SMT offlining if Active core control is enabled to be used in P1 or when performance control is applied.
ConfigTDP	[Disabled] <b>[Enabled]</b>	Enable/Disable Intel Configurable TDP. (Show as <u>SETUP_DATA.EnableSaDevice</u> is not 0 OR <u>SETUP_CPU_FEATURES.ConfigTdpAvailable</u> is not 0)
Intel(R) Dynamic Tuning Configuration	<b>minimum = 0</b> <b>maximum = 255</b> <b>step = 1</b> <b>default = 0</b>	An Integer containing the Intel(R) Dynamic Tuning Configuration bitmap: BIT0[Generic UI Access Control](0=enable,1=disable) BIT1[Restricted UI Access Control](0=enable,1=disable) BIT2[shell Access Control](0=enable,1=disable) BIT3[Environment Monitoring Report Control](0=report,1=silent) BIT4[Thermal Mitigation Report Control](0=silent,1=report) BIT5[Thermal Policy Report Control](0=silent,1=report)
FAN1 Device	[Disabled] <b>[Enabled]</b>	Enable the Fan1 device.
Display participant	<b>[Disabled]</b> [Enabled]	Enable/Disable the Display participant.

Display Low Limit	<b>minimum = 0</b> <b>maximum = 100</b> <b>step = 1</b> <b>default = 30</b>	Display Low Limit
Display High Limit	<b>minimum = 0</b> <b>maximum = 100</b> <b>step = 1</b> <b>default = 100</b>	Display High Limit - Between 0% to 100%
Wireless participant	<b>[Disabled]</b> [Enabled]	Enable/Disable the Wireless participant.
<u>(Below options will show at Wireless participant set enabled.)</u>		
Active Thermal Trip Point	<b>minimum = 0</b> <b>maximum = 127</b> <b>step = 1</b> <b>default = 63</b>	This value controls the temperature of the ACPI Active Thermal Trip Point. NOTE: a value of zero will cause the Intel Dynamic Tuning driver to disable the trip point.
Passive Thermal Trip Point	<b>minimum = 0</b> <b>maximum = 127</b> <b>step = 1</b> <b>default = 71</b>	This value controls the temperature of the ACPI Passive Thermal Trip Point. NOTE: a value of zero will cause the Intel Dynamic Tuning driver to disable the trip point.
Critical Thermal Trip Point	<b>minimum = 0</b> <b>maximum = 127</b> <b>step = 1</b> <b>default = 100</b>	This value controls the temperature of the ACPI Critical Thermal Trip Point. NOTE: a value of zero will cause the Intel Dynamic Tuning driver to disable the trip point.
S3/CS Thermal Trip Point	<b>minimum = 0</b> <b>maximum = 127</b> <b>step = 1</b> <b>default = 90</b>	This value controls the temperature of the ACPI Critical Thermal Trip Point for entering S3 or CS. NOTE: a value of zero will cause the Intel Dynamic Tuning driver to disable the trip point.
Hot Thermal Trip Point	<b>minimum = 0</b> <b>maximum = 127</b> <b>step = 1</b> <b>default = 95</b>	This value controls the temperature of the ACPI Hot Thermal Trip Point. NOTE: a value of zero will cause the Intel Dynamic Tuning driver to disable the trip point.
Thermal Sampling Period	<b>minimum = 0</b> <b>maximum = 100</b> <b>step = 1</b> <b>default = 0</b>	The polling interval in 10ths of seconds. A value of 0 tells the driver to use interrupts. NOTE: The granularity of the sampling period is 0.1 seconds. For example, if the sampling period is 30 seconds, then _TSP needs to report 300; if the sampling period is 0.5 seconds, then choose 5.
WWAN participant	<b>[Disabled]</b> [Enabled]	Enable/Disable the WWAN participant.
<u>(Below options will show at WWAN participant set enabled.)</u>		
Active Thermal Trip Point	<b>minimum = 0</b> <b>maximum = 127</b> <b>step = 1</b>	This value controls the temperature of the ACPI Active Thermal Trip Point.

	<b>default = 63</b>	NOTE: a value of zero will cause the Intel Dynamic Tuning driver to disable the trip point.
Passive Thermal Trip Point	<b>minimum = 0</b> <b>maximum = 127</b> <b>step = 1</b> <b>default = 71</b>	This value controls the temperature of the ACPI Passive Thermal Trip Point. NOTE: a value of zero will cause the Intel Dynamic Tuning driver to disable the trip point.
Critical Thermal Trip Point	<b>minimum = 0</b> <b>maximum = 127</b> <b>step = 1</b> <b>default = 100</b>	This value controls the temperature of the ACPI Critical Thermal Trip Point. NOTE: a value of zero will cause the Intel Dynamic Tuning driver to disable the trip point.
S3/CS Thermal Trip Point	<b>minimum = 0</b> <b>maximum = 127</b> <b>step = 1</b> <b>default = 90</b>	This value controls the temperature of the ACPI Critical Thermal Trip Point for entering S3 or CS. NOTE: a value of zero will cause the Intel Dynamic Tuning driver to disable the trip point.
Hot Thermal Trip Point	<b>minimum = 0</b> <b>maximum = 127</b> <b>step = 1</b> <b>default = 95</b>	This value controls the temperature of the ACPI Hot Thermal Trip Point. NOTE: a value of zero will cause the Intel Dynamic Tuning driver to disable the trip point.
Charger participant	<b>[Disabled]</b> [Enabled]	Enable/Disable Charger device
Power participant	<b>[Disabled]</b> [Enabled]	Enable/Disable the Power participant. (Below options will show at this options set enabled.)
Intel Dynamic Tuning Power Sampling Period	<b>minimum = 0</b> <b>maximum = 1000</b> <b>step = 1</b> <b>default = 0</b>	This power sampling period for the Power Participant Object.
2D Camera participant	<b>[Disabled]</b> [Enabled]	Enable/Disable the 2D Camera Participant.
Battery Participant	<b>[Disabled]</b> [Enabled]	Enable/Disable the Battery Participant.
Storage participant1	<b>[Disabled]</b> [Enabled]	Enable/Disable Storage device
<u>(Below options will show at this options set enabled.)</u>		
Active Thermal Trip Point	<b>minimum = 0</b> <b>maximum = 127</b> <b>step = 1</b> <b>default = 63</b>	This value controls the temperature of the ACPI Active Thermal Trip Point. NOTE: a value of zero will cause the Intel Dynamic Tuning driver to disable the trip point.
Passive Thermal Trip Point	<b>minimum = 0</b> <b>maximum = 127</b> <b>step = 1</b> <b>default = 71</b>	This value controls the temperature of the ACPI Passive Thermal Trip Point. NOTE: a value of zero will cause the Intel Dynamic Tuning driver to disable the trip point.

Critical Thermal Trip Point	<b>minimum = 0</b> <b>maximum = 127</b> <b>step = 1</b> <b>default = 100</b>	This value controls the temperature of the ACPI Critical Thermal Trip Point. NOTE: a value of zero will cause the Intel Dynamic Tuning driver to disable the trip point.
S3/CS Thermal Trip Point	<b>minimum = 0</b> <b>maximum = 127</b> <b>step = 1</b> <b>default = 90</b>	This value controls the temperature of the ACPI Critical Thermal Trip Point for entering S3 or CS. NOTE: a value of zero will cause the Intel Dynamic Tuning driver to disable the trip point.
Hot Thermal Trip Point	<b>minimum = 0</b> <b>maximum = 127</b> <b>step = 1</b> <b>default = 95</b>	This value controls the temperature of the ACPI Hot Thermal Trip Point. NOTE: a value of zero will cause the Intel Dynamic Tuning driver to disable the trip point.
Storage participant2	[Disabled] [Enabled]	Enable/Disable Storage device
<u>(Below options will show at this options set enabled.)</u>		
Active Thermal Trip Point	<b>minimum = 0</b> <b>maximum = 127</b> <b>step = 1</b> <b>default = 63</b>	This value controls the temperature of the ACPI Active Thermal Trip Point. NOTE: a value of zero will cause the Intel Dynamic Tuning driver to disable the trip point.
Passive Thermal Trip Point	<b>minimum = 0</b> <b>maximum = 127</b> <b>step = 1</b> <b>default = 71</b>	This value controls the temperature of the ACPI Passive Thermal Trip Point. NOTE: a value of zero will cause the Intel Dynamic Tuning driver to disable the trip point.
Critical Thermal Trip Point	<b>minimum = 0</b> <b>maximum = 127</b> <b>step = 1</b> <b>default = 100</b>	This value controls the temperature of the ACPI Critical Thermal Trip Point. NOTE: a value of zero will cause the Intel Dynamic Tuning driver to disable the trip point.
S3/CS Thermal Trip Point	<b>minimum = 0</b> <b>maximum = 127</b> <b>step = 1</b> <b>default = 90</b>	This value controls the temperature of the ACPI Critical Thermal Trip Point for entering S3 or CS. NOTE: a value of zero will cause the Intel Dynamic Tuning driver to disable the trip point.
Hot Thermal Trip Point	<b>minimum = 0</b> <b>maximum = 127</b> <b>step = 1</b> <b>default = 95</b>	This value controls the temperature of the ACPI Hot Thermal Trip Point. NOTE: a value of zero will cause the Intel Dynamic Tuning driver to disable the trip point.
Virtual Sensor participant 1	[Disabled] [Enabled]	Enable/Disable Virtual Sensor device.
<u>(Below options will show at this options set enabled.)</u>		
Active Thermal Trip Point	<b>minimum = 0</b> <b>maximum = 127</b> <b>step = 1</b>	This value controls the temperature of the ACPI Active Thermal Trip Point.

	<b>default = 50</b>	NOTE: a value of zero will cause the Intel Dynamic Tuning driver to disable the trip point.
Passive Thermal Trip Point	<b>minimum = 0</b> <b>maximum = 127</b> <b>step = 1</b> <b>default = 50</b>	This value controls the temperature of the ACPI Passive Thermal Trip Point. NOTE: a value of zero will cause the Intel Dynamic Tuning driver to disable the trip point.
Critical Thermal Trip Point	<b>minimum = 0</b> <b>maximum = 127</b> <b>step = 1</b> <b>default = 70</b>	This value controls the temperature of the ACPI Critical Thermal Trip Point. NOTE: a value of zero will cause the Intel Dynamic Tuning driver to disable the trip point.
S3/CS Thermal Trip Point	<b>minimum = 0</b> <b>maximum = 127</b> <b>step = 1</b> <b>default = 65</b>	This value controls the temperature of the ACPI Critical Thermal Trip Point for entering S3 or CS. NOTE: a value of zero will cause the Intel Dynamic Tuning driver to disable the trip point.
Hot Thermal Trip Point	<b>minimum = 0</b> <b>maximum = 127</b> <b>step = 1</b> <b>default = 60</b>	This value controls the temperature of the ACPI Hot Thermal Trip Point. NOTE: a value of zero will cause the Intel Dynamic Tuning driver to disable the trip point.
Virtual Sensor participant 2	<b>[Disabled]</b> [Enabled]	Enable/Disable Virtual Sensor device.
<u>(Below options will show at this options set enabled.)</u>		
Active Thermal Trip Point	<b>minimum = 0</b> <b>maximum = 127</b> <b>step = 1</b> <b>default = 50</b>	This value controls the temperature of the ACPI Active Thermal Trip Point. NOTE: a value of zero will cause the Intel Dynamic Tuning driver to disable the trip point.
Passive Thermal Trip Point	<b>minimum = 0</b> <b>maximum = 127</b> <b>step = 1</b> <b>default = 50</b>	This value controls the temperature of the ACPI Passive Thermal Trip Point. NOTE: a value of zero will cause the Intel Dynamic Tuning driver to disable the trip point.
Critical Thermal Trip Point	<b>minimum = 0</b> <b>maximum = 127</b> <b>step = 1</b> <b>default = 70</b>	This value controls the temperature of the ACPI Critical Thermal Trip Point. NOTE: a value of zero will cause the Intel Dynamic Tuning driver to disable the trip point.
S3/CS Thermal Trip Point	<b>minimum = 0</b> <b>maximum = 127</b> <b>step = 1</b> <b>default = 65</b>	This value controls the temperature of the ACPI Critical Thermal Trip Point for entering S3 or CS. NOTE: a value of zero will cause the Intel Dynamic Tuning driver to disable the trip point.
Hot Thermal Trip Point	<b>minimum = 0</b> <b>maximum = 127</b> <b>step = 1</b>	This value controls the temperature of the ACPI Hot Thermal Trip Point. NOTE:

	<b>default = 60</b>	a value of zero will cause the Intel Dynamic Tuning driver to disable the trip point.
Sensor Device 1	<b>[Disabled]</b> [Enabled]	Enable/Disable Sensor 1 device. (Show as SETUP_DATA.EnableSen1ParticipantSupport is 1)
<u>(Below options will show at this options set enabled.)</u>		
Active Thermal Trip Point	<b>minimum = 0</b> <b>maximum = 127</b> <b>step = 1</b> <b>default = 63</b>	This value controls the temperature of the ACPI Active Thermal Trip Point. NOTE: a value of zero will cause the Intel Dynamic Tuning driver to disable the trip point.
Passive Thermal Trip Point	<b>minimum = 0</b> <b>maximum = 127</b> <b>step = 1</b> <b>default = 71</b>	This value controls the temperature of the ACPI Passive Thermal Trip Point. NOTE: a value of zero will cause the Intel Dynamic Tuning driver to disable the trip point.
Critical Thermal Trip Point	<b>minimum = 0</b> <b>maximum = 127</b> <b>step = 1</b> <b>default = 103</b>	This value controls the temperature of the ACPI Critical Thermal Trip Point. NOTE: a value of zero will cause the Intel Dynamic Tuning driver to disable the trip point.
S3/CS Thermal Trip Point	<b>minimum = 0</b> <b>maximum = 127</b> <b>step = 1</b> <b>default = 97</b>	This value controls the temperature of the ACPI Critical Thermal Trip Point for entering S3 or CS. NOTE: a value of zero will cause the Intel Dynamic Tuning driver to disable the trip point.
Hot Thermal Trip Point	<b>minimum = 0</b> <b>maximum = 127</b> <b>step = 1</b> <b>default = 100</b>	This value controls the temperature of the ACPI Hot Thermal Trip Point. NOTE: a value of zero will cause the Intel Dynamic Tuning driver to disable the trip point.
Thermal Sampling Period	<b>minimum = 0</b> <b>maximum = 100</b> <b>step = 1</b> <b>default = 0</b>	The polling interval in 10ths of seconds. A value of 0 tells the driver to use interrupts. NOTE: The granularity of the sampling period is 0.1 seconds. For example, if the sampling period is 30 seconds, then _TSP needs to report 300; if the sampling period is 0.5 seconds, then choose 5.
Sensor Device 2	<b>[Disabled]</b> [Enabled]	Enable/Disable Sensor 2 device.
<u>(Below options will show at this options set enabled.)</u>		
Active Thermal Trip Point	<b>minimum = 0</b> <b>maximum = 127</b> <b>step = 1</b> <b>default = 60</b>	This value controls the temperature of the ACPI Active Thermal Trip Point. NOTE: a value of zero will cause the Intel Dynamic Tuning driver to disable the trip point.

Passive Thermal Trip Point	<b>minimum = 0</b> <b>maximum = 127</b> <b>step = 1</b> <b>default = 65</b>	This value controls the temperature of the ACPI Passive Thermal Trip Point. NOTE: a value of zero will cause the Intel Dynamic Tuning driver to disable the trip point.
Critical Thermal Trip Point	<b>minimum = 0</b> <b>maximum = 127</b> <b>step = 1</b> <b>default = 80</b>	This value controls the temperature of the ACPI Critical Thermal Trip Point. NOTE: a value of zero will cause the Intel Dynamic Tuning driver to disable the trip point.
S3/CS Thermal Trip Point	<b>minimum = 0</b> <b>maximum = 127</b> <b>step = 1</b> <b>default = 70</b>	This value controls the temperature of the ACPI Critical Thermal Trip Point for entering S3 or CS. NOTE: a value of zero will cause the Intel Dynamic Tuning driver to disable the trip point.
Hot Thermal Trip Point	<b>minimum = 0</b> <b>maximum = 127</b> <b>step = 1</b> <b>default = 75</b>	This value controls the temperature of the ACPI Hot Thermal Trip Point. NOTE: a value of zero will cause the Intel Dynamic Tuning driver to disable the trip point.
Thermal Sampling Period	<b>minimum = 0</b> <b>maximum = 100</b> <b>step = 1</b> <b>default = 0</b>	The polling interval in 10ths of seconds. A value of 0 tells the driver to use interrupts. NOTE: The granularity of the sampling period is 0.1 seconds. For example, if the sampling period is 30 seconds, then _TSP needs to report 300; if the sampling period is 0.5 seconds, then choose 5.
Sensor Device 3	[Disabled] [Enabled]	Enable/Disable Sensor 3 device.
<u>(Below options will show at this options set enabled.)</u>		
Active Thermal Trip Point	<b>minimum = 0</b> <b>maximum = 127</b> <b>step = 1</b> <b>default = 60</b>	This value controls the temperature of the ACPI Active Thermal Trip Point. NOTE: a value of zero will cause the Intel Dynamic Tuning driver to disable the trip point.
Passive Thermal Trip Point	<b>minimum = 0</b> <b>maximum = 127</b> <b>step = 1</b> <b>default = 65</b>	This value controls the temperature of the ACPI Passive Thermal Trip Point. NOTE: a value of zero will cause the Intel Dynamic Tuning driver to disable the trip point.
Critical Thermal Trip Point	<b>minimum = 0</b> <b>maximum = 127</b> <b>step = 1</b> <b>default = 80</b>	This value controls the temperature of the ACPI Critical Thermal Trip Point. NOTE: a value of zero will cause the Intel Dynamic Tuning driver to disable the trip point.
S3/CS Thermal Trip Point	<b>minimum = 0</b> <b>maximum = 127</b> <b>step = 1</b> <b>default = 70</b>	This value controls the temperature of the ACPI Critical Thermal Trip Point for entering S3 or CS. NOTE: a value of zero will cause the Intel Dynamic Tuning driver to disable the trip point.

Hot Thermal Trip Point	<b>minimum = 0</b> <b>maximum = 127</b> <b>step = 1</b> <b>default = 75</b>	This value controls the temperature of the ACPI Hot Thermal Trip Point. NOTE: a value of zero will cause the Intel Dynamic Tuning driver to disable the trip point.
Thermal Sampling Period	<b>minimum = 0</b> <b>maximum = 100</b> <b>step = 1</b> <b>default = 0</b>	The polling interval in 10ths of seconds. A value of 0 tells the driver to use interrupts. NOTE: The granularity of the sampling period is 0.1 seconds. For example, if the sampling period is 30 seconds, then _TSP needs to report 300; if the sampling period is 0.5 seconds, then choose 5.
Sensor Device 4	<b>[Disabled]</b> [Enabled]	Enable/Disable Sensor 4 device.
<u>(Below options will show at this options set enabled.)</u>		
Active Thermal Trip Point	<b>minimum = 0</b> <b>maximum = 127</b> <b>step = 1</b> <b>default = 60</b>	This value controls the temperature of the ACPI Active Thermal Trip Point. NOTE: a value of zero will cause the Intel Dynamic Tuning driver to disable the trip point.
Passive Thermal Trip Point	<b>minimum = 0</b> <b>maximum = 127</b> <b>step = 1</b> <b>default = 65</b>	This value controls the temperature of the ACPI Passive Thermal Trip Point. NOTE: a value of zero will cause the Intel Dynamic Tuning driver to disable the trip point.
Critical Thermal Trip Point	<b>minimum = 0</b> <b>maximum = 127</b> <b>step = 1</b> <b>default = 80</b>	This value controls the temperature of the ACPI Critical Thermal Trip Point. NOTE: a value of zero will cause the Intel Dynamic Tuning driver to disable the trip point.
S3/CS Thermal Trip Point	<b>minimum = 0</b> <b>maximum = 127</b> <b>step = 1</b> <b>default = 70</b>	This value controls the temperature of the ACPI Critical Thermal Trip Point for entering S3 or CS. NOTE: a value of zero will cause the Intel Dynamic Tuning driver to disable the trip point.
Hot Thermal Trip Point	<b>minimum = 0</b> <b>maximum = 127</b> <b>step = 1</b> <b>default = 75</b>	This value controls the temperature of the ACPI Hot Thermal Trip Point. NOTE: a value of zero will cause the Intel Dynamic Tuning driver to disable the trip point.
Thermal Sampling Period	<b>minimum = 0</b> <b>maximum = 100</b> <b>step = 1</b> <b>default = 0</b>	The polling interval in 10ths of seconds. A value of 0 tells the driver to use interrupts. NOTE: The granularity of the sampling period is 0.1 seconds. For example, if the sampling period is 30 seconds, then _TSP needs to report 300; if the sampling period is 0.5 seconds, then choose 5.
Sensor Device 5	<b>[Disabled]</b> [Enabled]	Enable/Disable Sensor 5 device.
<u>(Below options will show at this options set enabled.)</u>		

Active Thermal Trip Point	<b>minimum = 0</b> <b>maximum = 127</b> <b>step = 1</b> <b>default = 60</b>	This value controls the temperature of the ACPI Active Thermal Trip Point. NOTE: a value of zero will cause the Intel Dynamic Tuning driver to disable the trip point.
Passive Thermal Trip Point	<b>minimum = 0</b> <b>maximum = 127</b> <b>step = 1</b> <b>default = 65</b>	This value controls the temperature of the ACPI Passive Thermal Trip Point. NOTE: a value of zero will cause the Intel Dynamic Tuning driver to disable the trip point.
Critical Thermal Trip Point	<b>minimum = 0</b> <b>maximum = 127</b> <b>step = 1</b> <b>default = 80</b>	This value controls the temperature of the ACPI Critical Thermal Trip Point. NOTE: a value of zero will cause the Intel Dynamic Tuning driver to disable the trip point.
S3/CS Thermal Trip Point	<b>minimum = 0</b> <b>maximum = 127</b> <b>step = 1</b> <b>default = 70</b>	This value controls the temperature of the ACPI Critical Thermal Trip Point for entering S3 or CS. NOTE: a value of zero will cause the Intel Dynamic Tuning driver to disable the trip point.
Hot Thermal Trip Point	<b>minimum = 0</b> <b>maximum = 127</b> <b>step = 1</b> <b>default = 75</b>	This value controls the temperature of the ACPI Hot Thermal Trip Point. NOTE: a value of zero will cause the Intel Dynamic Tuning driver to disable the trip point.
Thermal Sampling Period	<b>minimum = 0</b> <b>maximum = 100</b> <b>step = 1</b> <b>default = 0</b>	The polling interval in 10ths of seconds. A value of 0 tells the driver to use interrupts. NOTE: The granularity of the sampling period is 0.1 seconds. For example, if the sampling period is 30 seconds, then _TSP needs to report 300; if the sampling period is 0.5 seconds, then choose 5.
OEM variable and Object	(See section 2.2.17.3.1)	OEM variable and Object options. (Show as <code>SETUP_DATA.EnableDptf</code> is not 0)

### 2.2.19.3.1 OEM variable and Object

**Table 2-2-19-3-1. OEM variable and Object**

BIOS Setting	Options	Description
OEM variable and Object		
Design Variable 0	<b>minimum = 0</b> <b>maximum = 255</b> <b>step = 1</b> <b>default = 0</b>	OEM Design Variable: an integer between 0-255. This allows OEM's to customize Intel Dynamic Tuning behavior based on platform changes.
Design Variable 1		
Design Variable 2		
Design Variable 3		
Design Variable 4		

Design Variable 5		
PPCC Object	[Disabled] <b>[Enabled]</b>	Enable/Disable PPCC object for validation.
PDRT Object	[Disabled] <b>[Enabled]</b>	Enable/Disable PDRT object for validation.
ARTG Object	[Disabled] <b>[Enabled]</b>	Enable/Disable ARTG object for validation.
PMAX Object	<b>[Disabled]</b> [Enabled]	Enable/Disable PMAX object for validation.
Processor Thermal Device	No options	Intel(R) Dynamic Tuning Configuration options
_TMP 1 Object	<b>[Disabled]</b> [Enabled]	Enable/Disable _TMP 1 object for validation.

### 2.2.19.4 Hardware Health Monitor

**Table 2-2-19-4. Hardware Health Monitor**

BIOS Setting	Options	Description
Hardware Health Monitor		
<u>(Below options are gray out.)</u>		
Thermal Sensor 1 Temp	No options	Help on Thermal Sensor 1 Temp.
Thermal Sensor 2 Temp	No options	Help on Thermal Sensor 2 Temp.
Thermal Sensor 3 Temp	No options	Help on Thermal Sensor 3 Temp.
Thermal Sensor 4 Temp	No options	Help on Thermal Sensor 4 Temp.
Thermal Sensor 5 Temp	No options	Help on Thermal Sensor 5 Temp.
CPU Fan Speed	No options	Help on CPU Fan.
PCH DTS Temp from PCH	No options	Help on PCH DTS Temp

### 2.2.20 Platform Settings

**Table 2-2-20. Platform Settings**

BIOS Setting	Options	Description
Platform Settings		
Charging Method	<b>[Normal Charging]</b> [Fast Charging]	Select charging method as Normal Charging or Fast Charging.
Pseudo G3		Enable/Disable Pseudo G3

PS2 Keyboard and Mouse	[Disabled] <b>[Enabled]</b>	Enables/Disables PS2 Keyboard and Mouse.
EC PECI Mode	[Legacy PECI mode] <b>[PECI over eSPI mode]</b>	Switch eSPI PECI Mode or Legacy PECI mode
Power Loss Notification Feature	[Disabled] [Enabled] <b>[Default]</b>	Enable/Disable Power Loss Notification Feature
Device password support	[Disabled] <b>[Enabled]</b>	Support device password feature
Pmic Vcc IO Level	<b>[Disabled]</b> [1.05V] [1.071V] [1.023V] [0.997V] [0.850V] [0.900V] [0.950V]	Select the Pmic Vcc IO Voltage Level.
Pmic Vddq Level	<b>[Disabled]</b> [0] [1] [2] [3] [4] [5] [6] [7]	Select the Pmic Vddq Voltage Level.
CSC Pmic NVM Update Support	<b>[Disabled]</b> [Enabled]	Enable/Disable CastroCove Pmic Nvm Update <i>(Below will show at this set Enable)</i>
CSC Pmic Customization Nvm Update Support	<b>[Disabled]</b> [Enabled]	Enable/Disable CastroCove Pmic Customization Nvm Update
Pmic NVM Write Lock Support	<b>[Disabled]</b> [Enabled]	Enable/Disable WarrenCove/CastroCove Pmic Nvm Write Lock
HEBC value	<b>minimum = 0</b> <b>maximum = 0xFFFFFFFF</b> <b>step = 1</b> <b>default = 0x233F3</b>	HEBC value 32bit.
Pmic SlpS0 VM Support	<b>[Disabled]</b> [Enabled]	Support to auto check Primium PMIC and disable SlpS0 voltage.
Power Sharing Manager	<b>[Disabled]</b> [Enabled]	Configure the PSM ACPI objects. <i>(Below will show at this set Enable)</i>
Domain Type SPLC 1	<b>minimum = 1</b> <b>maximum = 50</b> <b>step = 1</b> <b>default = 9</b>	09h: Module(M.2); 07h: WiFi/WLAN; 0Fh: WWAN; 10h: WiGig; 14h: RFEM
Default Power Limit 1 SPLC	<b>minimum = 1</b> <b>maximum = 10000</b> <b>step = 1</b> <b>default = 4000</b>	Power Limit in milli watts
Default Time Window 1 SPLC	<b>minimum = 1</b> <b>maximum = 100000</b> <b>step = 1</b> <b>default = 30000</b>	Time Window in milli seconds
Domain Type DPLC 1	<b>minimum = 1</b> <b>maximum = 50</b> <b>step = 1</b> <b>default = 9</b>	09h: Module(M.2); 07h: WiFi/WLAN; 0Fh: WWAN; 10h: WiGig; 14h: RFEM

Domain Preference DPLC 1	<b>minimum = 1</b> <b>maximum = 50</b> <b>step = 1</b> <b>default = 9</b>	09h: Module(M.2); 07h: WiFi/WLAN; 0Fh: WWAN; 10h WiGig; 14h: RFEM
Power Limit Index 1 DPLC	<b>minimum = 0</b> <b>maximum = 10</b> <b>step = 1</b> <b>default = 0</b>	Index of the specific power limit range information
Default Power Limit 1 DPLC	<b>minimum = 1</b> <b>maximum = 10000</b> <b>step = 1</b> <b>default = 1200</b>	Power Limit in milli watts
Default Time Window 1 DPLC	<b>minimum = 1</b> <b>maximum = 100000</b> <b>step = 1</b> <b>default = 30000</b>	Time Window in milli seconds
Minimum Power Limit 1 DPLC	<b>minimum = 1</b> <b>maximum = 10000</b> <b>step = 1</b> <b>default = 1200</b>	Power Limit in milli watts
Maximum Power Limit 1 DPLC	<b>minimum = 1</b> <b>maximum = 10000</b> <b>step = 1</b> <b>default = 1200</b>	Power Limit in milli watts
Maximum Time Window 1 DPLC	<b>minimum = 1</b> <b>maximum = 10000</b> <b>step = 1</b> <b>default = 1000</b>	Time Window in milli seconds
Enable FFU Support	<b>[Disabled]</b> [Enabled]	Enable/Disable FFU Support.
Delay to wait for WWAN device to be ready before SAR reset.	<b>minimum = 0</b> <b>maximum = 255</b> <b>step = 1</b> <b>default = 8</b>	Value between 0-255 seconds. Will result in Responsiveness impact.
HID Event Filter Driver	[Disabled] <b>[Enabled]</b>	Enables/Disables HID Event Filter Driver interface to OS.
System Time and Alarm Source	<b>[ACPI Time and Alarm Device]</b> [Legacy RTC]	Select source of system time and alarm functions. ACPI Time and Alarm (default, legacy RTC disabled) or Legacy RTC support only.
DG Platform Support	<b>[Add In Card]</b> [MB Down]	DG is supported as MotherBoard Down OR Add In Card
Enable PowerMeter	<b>[Disabled]</b> [Enabled]	Enables/Disables PowerMeter.
Intel Trusted Device Setup Boot	[Enabled] <b>[Disabled]</b>	Enables/Disables a Intel Trusted Device Setup Boot on the next boot
MPDT Support	<b>[Disabled]</b> [Sensor_BOM1]	Enable(Sensor_BOM1,Sensor_BOM2 and Sensor_BOM1 with Companion

	[Sensor_BOM2] [Sensor_BOM1 with Companion Chip]	Chip)/Disable MPDT Support in BIOS
Closed Lid WoV LED Lighting Support	<b>[Disabled]</b> [Enabled]	Disables/Enables Closed Lid WoV LED Lighting Support.
System Firmware Update Config	(See section 2.2.20.1)	Config settings for System Firmware Update (Capsule Update).
VTIO	(See section 2.2.20.2)	Configure settings for VTIO.
TCSS Platform Setting	(See section 2.2.20.3)	Configure TCSS Platform Setting

### 2.2.20.1 System Firmware Update Config

**Table 2-2-20-1. System Firmware Update Config**

BIOS Setting	Options	Description
System Firmware Update Config		
Restore Setup Default	<b>[Disabled]</b> [Enabled]	Restore Setup default settings after System Firmware Update.
Skip Power Check	<b>[Disabled]</b> [Enabled]	Skip AC/DC Check before System Firmware Update.

## 2.2.20.2 VTIO

**Table 2-2-20-2. VTIO**

BIOS Setting	Options	Description
VTIO		
Enable VTIO Support	<b>[Disabled]</b> [Enabled]	Enable/Disable VTIO Support.
Expose ISP SDEV Entry	[Disabled] <b>[Enabled]</b>	ISP Entry in SDEV table will be exposed based on this option. (Below options will show at this options set enabled.)
Number of Sensor Entries	<b>minimum = 0</b> <b>maximum = 0x2</b> <b>step = 0</b> <b>default = 0x2</b>	An array of Sensors Entries.
Sensor Entry 1	<b>minimum = 0</b> <b>maximum = 0xFFFF</b> <b>step = 0</b> <b>default = 0x1</b>	Enter HEX value BIT0 - Embedded Sensor present BIT1 - Privacy Enabled Sensor present BIT5:2 - Port ID BIT6 - Plug-N-Play supported BIT8:7 - Camera type
Sensor Entry 2	<b>minimum = 0</b> <b>maximum = 0xFFFF</b> <b>step = 0</b> <b>default = 0x85</b>	Enter HEX value BIT0 - Embedded Sensor present BIT1 - Privacy Enabled Sensor present BIT5:2 - Port ID BIT6 - Plug-N-Play supported BIT8:7 - Camera type
Expose HECI SDEV Entry	[Disabled] <b>[Enabled]</b>	HECI Entry in SDEV table will be exposed based on this option. (Below options will show at this options set enabled.)
Number of Sensor Entries	<b>minimum = 0</b> <b>maximum = 0x2</b> <b>step = 0</b> <b>default = 0</b>	An array of Sensors Entries.
Sensor Entry 1	<b>minimum = 0</b> <b>maximum = 0xFFFF</b> <b>step = 0</b> <b>default = 0</b>	Enter HEX value BIT0 - Embedded Sensor present BIT1 - Privacy Enabled Sensor present BIT5:2 - Port ID BIT6 - Plug-N-Play supported BIT8:7 - Camera type
Sensor Entry 2	<b>minimum = 0</b> <b>maximum = 0xFFFF</b> <b>step = 0</b> <b>default = 0</b>	Enter HEX value BIT0 - Embedded Sensor present BIT1 - Privacy Enabled Sensor present BIT5:2 - Port ID BIT6 - Plug-N-Play supported

		BIT8:7 - Camera type
Expose SPI1 Dev 1E Fun 2 SDEV Entry	[Disabled] <b>[Enabled]</b>	SPI1 Entry in SDEV table will be exposed based on this option. ( <u>Below options will show at this options set enabled.</u> )
Number of Sensor Entries	<b>minimum = 0</b> <b>maximum = 0x2</b> <b>step = 0</b> <b>default = 0x1</b>	An array of Sensors Entries.
Sensor Entry 1	<b>minimum = 0</b> <b>maximum = 0xFFFF</b> <b>step = 0</b> <b>default = 0x1</b>	Enter HEX value BIT0 - Embedded Sensor present BIT1 - Privacy Enabled Sensor present BIT5:2 - Port ID BIT6 - Plug-N-Play supported BIT8:7 - Camera type
Sensor Entry 2	<b>minimum = 0</b> <b>maximum = 0xFFFF</b> <b>step = 0</b> <b>default = 0</b>	Enter HEX value BIT0 - Embedded Sensor present BIT1 - Privacy Enabled Sensor present BIT5:2 - Port ID BIT6 - Plug-N-Play supported BIT8:7 - Camera type
Expose SPI2 Dev 1E Fun 3 SDEV Entry	[Disabled] <b>[Enabled]</b>	SPI2 Entry in SDEV table will be exposed based on this option. ( <u>Below options will show at this options set enabled.</u> )
Number of Sensor Entries	<b>minimum = 0</b> <b>maximum = 0x2</b> <b>step = 0</b> <b>default = 0x1</b>	An array of Sensors Entries.
Sensor Entry 1	<b>minimum = 0</b> <b>maximum = 0xFFFF</b> <b>step = 0</b> <b>default = 0x1</b>	Enter HEX value BIT0 - Embedded Sensor present BIT1 - Privacy Enabled Sensor present BIT5:2 - Port ID BIT6 - Plug-N-Play supported BIT8:7 - Camera type
Sensor Entry 2	<b>minimum = 0</b> <b>maximum = 0xFFFF</b> <b>step = 0</b> <b>default = 0</b>	Enter HEX value BIT0 - Embedded Sensor present BIT1 - Privacy Enabled Sensor present BIT5:2 - Port ID BIT6 - Plug-N-Play supported BIT8:7 - Camera type
Expose XHCI SDEV Entry	[Disabled] <b>[Enabled]</b>	XHCI Entry in SDEV table will be exposed based on this option ( <u>Below options will show at this options set enabled.</u> )

Number of USB Devices	<b>minimum = 0x1</b> <b>maximum = 0x2</b> <b>step = 0</b> <b>default = 0x2</b>	Number of USB Devices
USB Device 1		
Attributes	<b>minimum = 0</b> <b>maximum = 0xFF</b> <b>step = 0</b> <b>default = 0</b>	Enter HEX value BIT[7:1] - Reserved. BIT[0] - USB Composite Device 0x0 - A single interface USB device 0x1 - A function on a USB composite device
Root Port Number	<b>minimum = 0</b> <b>maximum = 0xFF</b> <b>step = 0</b> <b>default = 0</b>	Root port number on which the secure device is attached to the root hub.
VID	<b>minimum = 0</b> <b>maximum = 0xFFFF</b> <b>step = 0</b> <b>default = 0</b>	Vendor ID
PID	<b>minimum = 0</b> <b>maximum = 0xFFFF</b> <b>step = 0</b> <b>default = 0</b>	Product ID
Revision	<b>minimum = 0</b> <b>maximum = 0xFFFF</b> <b>step = 0</b> <b>default = 0</b>	Revision
Interface Number	<b>minimum = 0</b> <b>maximum = 0xFF</b> <b>step = 0</b> <b>default = 0</b>	Interface number (0-based) of the interface on the device that this entry corresponds to. This field is considered valid only if the Attributes indicates that the device is a composite device.
Class	<b>minimum = 0</b> <b>maximum = 0xFF</b> <b>step = 0</b> <b>default = 0xE</b>	Class Number of the secure device
Subclass	<b>minimum = 0</b> <b>maximum = 0xFF</b> <b>step = 0</b> <b>default = 0x1</b>	Subclass Number of the secure device
Protocol	<b>minimum = 0</b> <b>maximum = 0xFF</b> <b>step = 0</b> <b>default = 0x1</b>	Protocol Number of the secure device
ACPI Path String Offset	<b>minimum = 0</b> <b>maximum = 0xFFFF</b> <b>step = 0</b> <b>default = 0x34</b>	Offset for fully qualified ACPI path name of the secure device from the beginning of this table

ACPI Path String Length	<b>minimum = 0</b> <b>maximum = 0xFFFF</b> <b>step = 0</b> <b>default = 0x1D</b>	Length of fully qualified, null terminated ACPI path name of the secure device, The length includes the NULL terminator.
Firmware Hash [255:192]	<b>minimum = 0</b> <b>maximum = 0xFFFFFFFFFFFFFFFF</b> <b>step = 0x1</b> <b>default = 0x0</b>	Firmware Hash [255:192]
Firmware Hash [191:128]	<b>minimum = 0</b> <b>maximum = 0xFFFFFFFFFFFFFFFF</b> <b>step = 0x1</b> <b>default = 0x0</b>	Firmware Hash [191:128]
Firmware Hash [127:64]	<b>minimum = 0</b> <b>maximum = 0xFFFFFFFFFFFFFFFF</b> <b>step = 0x1</b> <b>default = 0x0</b>	Firmware Hash [127:64]
Firmware Hash [63:0]	<b>minimum = 0</b> <b>maximum = 0xFFFFFFFFFFFFFFFF</b> <b>step = 0x1</b> <b>default = 0x0</b>	Firmware Hash [63:0]
ACPI Path Name	<b>minimum = 1</b> <b>maximum = 48</b>	ACPI Path Name. The default value is: \\_SB.PCI0.XHC.RHUB.HS00.CRGB

### 2.2.20.3 TCSS Platform Setting

**Table 2-2-20-3. TCSS Platform Setting**

BIOS Setting	Options	Description
System Firmware Update Config		
Disable TBT PCIE Tree BME	<b>[Disabled]</b> [Enabled]	Disable TBT PCIE RP and child device Tree BME to Enable VTD Base Security
USBC connector manager selection	[Disabled] <b>[Enable UCSI Device]</b> [Enable UCMC Device]	Select UCSI or UCMC device in ACPI support based on configuration
Type C retimer TX Compliance Mode	<b>[Disabled]</b> [Enabled]	Default is disable Compliance Mode. Change to enabled for Type C retimer Tx Compliance Mode testing.
BIOS-TCSS handshake	<b>[Disabled]</b> [Enabled]	Enable/Disable BIOS TCSS handshake messages. \nDisabled: TCSS handshake disabled \nEnabled: TCSS handshake with

		either EC or PMC is enabled based on the board ID <i>(Below will show at this set Enable)</i>
Timeout for EC USB enumeration message	<b>minimum = 50</b> <b>maximum = 1000</b> <b>step = 10</b> <b>default = 50</b>	BIOS-EC handshake message USBC_GetUSBConnStatus timeout value in milli seconds
USBC and USBA Wake Capability	[S3] [S4]	USBC and USBA Wake Capability
USBC DataRole Swap Platform Disable Option	[TRUE] [FALSE]	Enable/Disable setting USBC DataRole Swap Platform Disable Option
Thunderbolt(TM) Configuration	(See section 2.2.20.3.1)	Thunderbolt(TM) Related Configuration
PD Information	No Options	
PD0 Version	No Options	PD0 Version
PD1 Version	No Options	PD1 Version

### 2.2.20.3.1 Thunderbolt(TM) Configuration

**Table 2-2-20-3-1. Thunderbolt(TM) Configuration**

BIOS Setting	Options	Description
Thunderbolt(TM) Configuration		
PCIe Tunneling over USB4	[Disabled] [Enabled]	Enable or disable PCIe Tunneling over USB4
USB4 CM Mode	[Firmware CM Only] [Software CM first] [OS Dependent] [CM Debug]	FW CM only - The system boots with FW CM only in both BIOS and OS phase. SW CM first - The system boots with SW CM in BIOS phase all the time, then boot to OS based on OS preference for backward and forward compatible. OS dependent - The system will boot with SW CM in BIOS phase after saving this setting, then boot to OS based on OS preference the reflect to CM setting to next BIOS boot. CM debug - The system with boot without any CM in BIOS phase, then boot to OS with the CM based on OS' preference by every boot.
Integrated Thunderbolt(TM) Support	[Disabled] [Enabled]	Enable or Disable Integrated Thunderbolt(TM) Support. <i>(Below will show at this set Enable)</i>

Wake From Thunderbolt(TM) Devices	[Disabled] <b>[Enabled]</b>	Enable or disable system wake from Thunderbolt(TM) devices.
Integrated Thunderbolt(TM) Configuration	(See section 2.2.20.3.1.1)	Integrated Thunderbolt(TM) Related Configuration

### 2.2.20.3.1.1 Integrated Thunderbolt(TM) Configuration

**Table 2-2-20-3-1-1. Integrated Thunderbolt(TM) Configuration**

BIOS Setting	Options	Description
Integrated Thunderbolt(TM) Configuration		
Os Native Resource Balance	<b>[Disabled]</b> [Enabled]	Os Native Resource Balance
Connect Topology Timeout value for ITBT	<b>minimum = 1 maximum = 65535 step = 1 default = 5000</b>	Connect Topology Timeout value for Integrated Thunderbolt(TM) Controller
Force Poweron Timeout value for ITBT	<b>minimum = 1 maximum = 65535 step = 1 default = 500</b>	Force Poweron Timeout value for Integrated Thunderbolt(TM)
ITBT RTD3	[Disabled] <b>[Enabled]</b>	ITBT RTD3 Enable/Disable. Note: ITBT RTD3 Disabled is not supported when SW CM is applied for OS
ITBT RTD3 EXIT DELAY	<b>minimum = 0 maximum = 20000 step = 1 default = 0</b>	ITBT RTD3 EXIT DELAY (milli seconds)

### 2.2.21 ACPI D3Cold settings

**Table 2-2-21. ACPI D3Cold settings**

BIOS Setting	Options	Description
ACPI D3Cold settings		
ACPI D3Cold Support	[Disabled] <b>[Enabled]</b>	Enable/Disable ACPI D3Cold (RTD3) support. <u>(Below options will show at this options set enabled.)</u>
VR Ramp up delay	<b>minimum = 0 maximum = 100 step = 16 default = 16</b>	Delay between subsequent VR ramp ups if they are all Turn ON at the same time.
PCIE Slot 5 Device Power-on delay in ms	<b>minimum = 0 maximum = 100 step = 16</b>	Delay between applying core power and Deasserting PERST#

	<b>default = 100</b>	
Audio Delay	<b>minimum = 0</b> <b>maximum = 1000</b> <b>step = 16</b> <b>default = 200</b>	Delay after applying power to HD Audio(Realtek) codec device. (Show as <i>PCH_SETUP.PchHdAudio</i> is not 0)
SensorHub	<b>minimum = 0</b> <b>maximum = 1000</b> <b>step = 16</b> <b>default = 68</b>	Delay after applying power to SensorHub device.
TouchPad	<b>minimum = 0</b> <b>maximum = 1000</b> <b>step = 16</b> <b>default = 68</b>	Delay after applying power to TouchPad device.
TouchPanel	<b>minimum = 0</b> <b>maximum = 1000</b> <b>step = 16</b> <b>default = 68</b>	Delay in PR_ON after applying power to TouchPanel device.
P-state Capping	<b>[Disabled]</b> [Enabled]	Set _PPC and send ACPI notification
USB Port 1	[High Speed] [Super Speed] <b>[Disabled]</b>	USB RTD3 support. Super Speed : USB3.0 devices will be exposed as RTD3 capable. High Speed: USB2.0 devices will be exposed as RTD3 capable. Disabled : USB RTD3 support disabled. For SawtoothPeak USB Port1(Below) is Superspeed and Port2(Top) is HighSpeed. Check respective board configuration to know about USB port position.
USB Port 2	SETUP_DATA.Rtd3WWAN is 0: <b>[Disabled]</b> [High Speed] [Super Speed]  else: <b>[Disabled]</b> [High Speed] [Super Speed] [Super Speed WWAN]	USB RTD3 support. Super Speed : USB3.0 devices will be exposed as RTD3 capable. High Speed: USB2.0 devices will be exposed as RTD3 capable. Disabled : USB RTD3 support disabled. For SawtoothPeak USB Port1(Below) is Superspeed and Port2(Top) is HighSpeed. Check respective board configuration to know about USB port position.
ZPODD	<b>[Disabled]</b> [Enabled]	Zero Power ODD option is applicable only for the board with ZPODD support.
WWAN	[Disable] <b>[D3/L2]</b> [D3/L1.2] [D0/L1.2]	Enable/Disable RTD3 support for WWAN.
ACPI D3Cold Support for Storage	[D3 Hot Enable/Disable] <b>[D3 Cold Enable/Disable]</b>	Enable/Disable RTD3 support for Storage. PCIE storage PEP constraint needs to be set as D0/F1

		(Intel Advanced -> ACPI Settings -> PEP PCIe Storage) when this setup is disabled
Sata Port 0	<b>[Disabled]</b> [Enabled]	Setup option to control the SATA port RTD3 functionality.
Sata Port 1	<b>[Disabled]</b> [Enabled]	
Sata Port 2	<b>[Disabled]</b> [Enabled]	
Sata Port 3	<b>[Disabled]</b> [Enabled]	
Sata Port 4	<b>[Disabled]</b> [Enabled]	
Sata Port 5	<b>[Disabled]</b> [Enabled]	
PCIe Remapped CR1	<b>[Disabled]</b> [Enabled]	PCIe RTD3 setup conflicts with SATA RTD3. Platform specific.
PCIe Remapped CR2	<b>[Disabled]</b> [Enabled]	
PCIe Remapped CR3	<b>[Disabled]</b> [Enabled]	
TBT Power-off delay in ms	<b>minimum = 0</b> <b>maximum = 15000</b> <b>step = 1</b> <b>default = 5000</b>	Specify delay in ms necessary after removing TBT power

## 2.2.22 BCLK Configuration

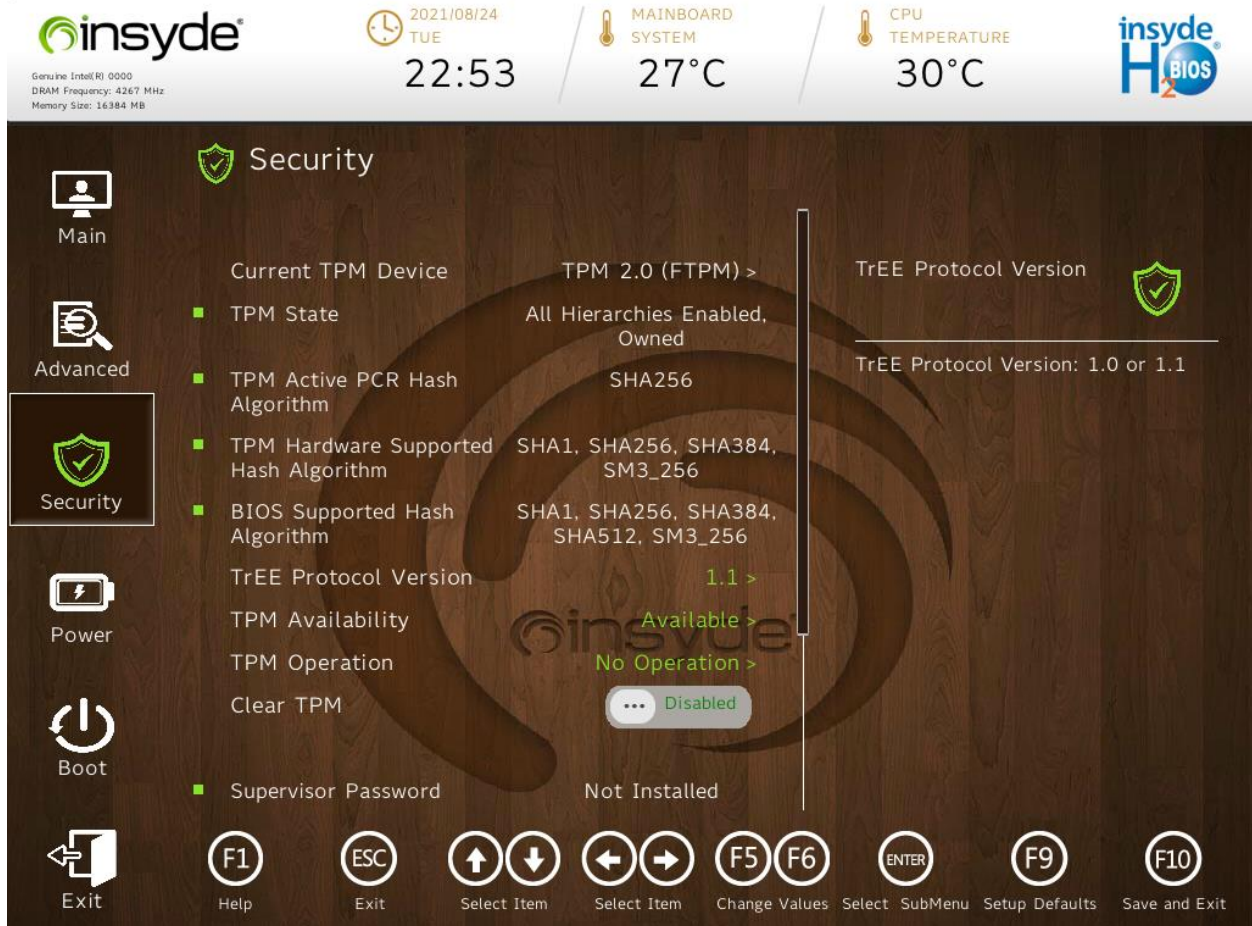
**Table 2-2-22. BCLK Configuration**

BIOS Setting	Options	Description
BCLK Configuration		
BCLK Source Config	<b>[CPU BCLK]</b>	CPU BCLK is only BCLK Source for ADL.
CPU - BCLK Clock Settings	No Options	
Bclk Frequency	No Options	

## 2.3 Security Menu

Security Menu of InsydeH2O BIOS Setup Utility provides configurations for the security settings of the system.

**Figure 2-3. Setup Utility Security Menu**



Note: If there is no TPM device on platform, TPM status is Not Installed, or it will be Enabled and Active.

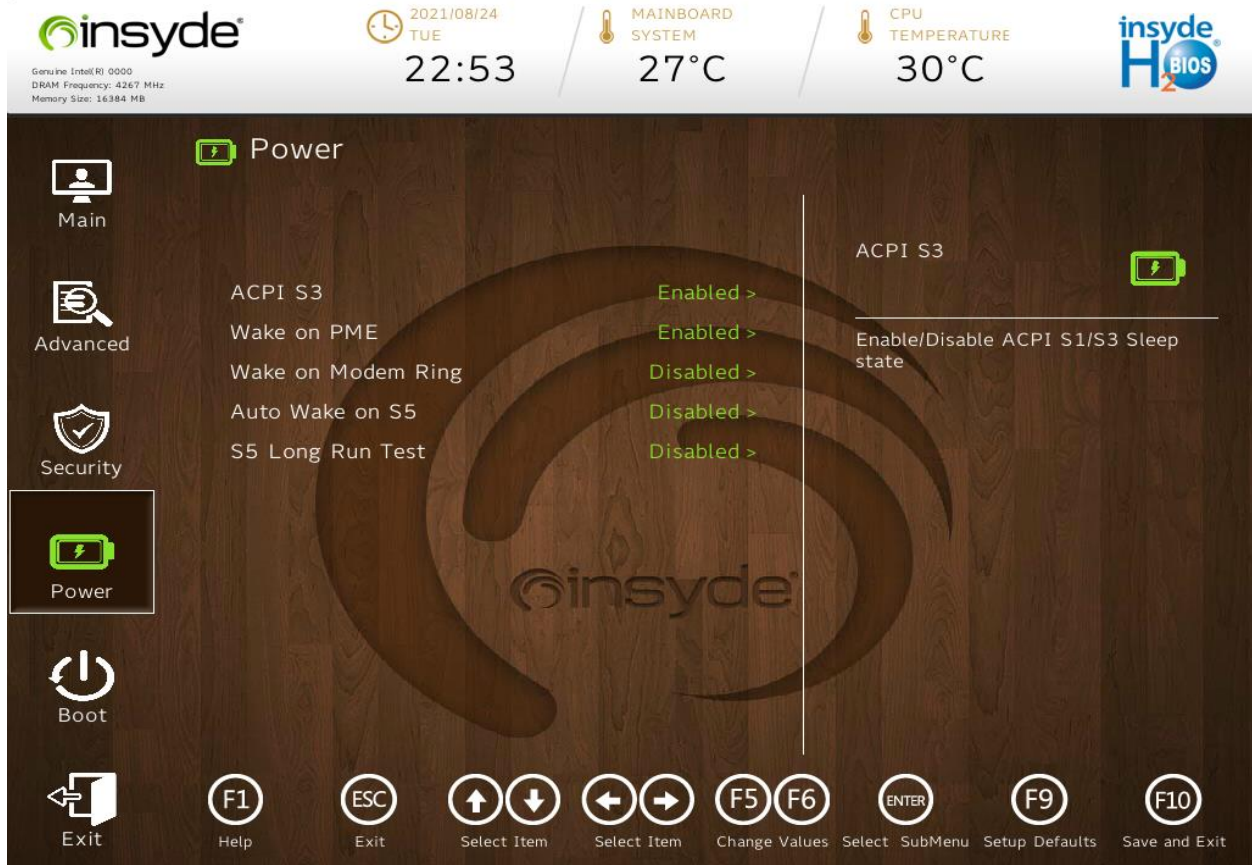
**Table 2-3 Security**

BIOS Setting		Options	Description
Current TPM Device		[TPM 1.2] <b>[TPM 2.0]</b>	Current TPM Device: TPM 1.2, or TPM2.0.
TPM State		All Hierarchies Enabled, Owned	
TPM Active PCR Hash Algorithm		SHA256	TPM Active PCR Hash Algorithm: SHA1, SHA256, SHA384, SHA512, SM3_256
TPM Hardware Supported Hash Algorithm		SHA1, SHA256, SHA384, SM3_256	TPM Hardware Supported Hash Algorithm: SHA1, SHA256, SHA384, SHA512, SM3_256
BIOS Supported Hash Algorithm		SHA1, SHA256, SHA384, SHA512, SM3_256	BIOS Supported Hash Algorithm: SHA1, SHA256, SHA384, SHA512, SM3_256
c	TrEE Protocol Version	[1.0] <b>[1.1]</b>	TrEE Protocol Version: 1.0 or 1.1
	TPM Availability	<b>[Available]</b> [Hidden]	When Hidden, don't exposes TPM to OS (Show at TPM device on platform or PTT Support Enable)
	TPM Operation	<b>[No Operation]</b> [Disabled] [Enabled]	Enable: Enable Storage and Endorsement Hierarchy. Disable: Disable Storage and Endorsement Hierarchy. (Show at TPM device on platform or PTT Support Enable)
	Clear TPM	<b>[Disabled]</b> [Enabled]	Clear TPM. Removes all TPM context associated with a specific Owner.
Supervisor Password		No options	When set password is enabled, you will be asked to input a Supervisor Password of your liking.
Set Supervisor Password		No options	Install or Change the password and the length of password must be greater than one character.

## 2.4 Power Menu

Power Menu of InsydeH2O Setup Utility allows users to set or control various parameters on CPU power management, and platform power management.

**Figure 2-4. Setup Utility Power Menu**



**Table 2-4 Power Menu setting**

BIOS Setting	Options	Description
ACPI S3	[Disabled] <b>[Enabled]</b>	Current TPM Device: TPM 1.2, or TPM2.0.
Wake on PME	[Disabled] <b>[Enabled]</b>	Determines the action taken when the system power is off and a PCI Power Management Enable wake up event occurs.
Wake on Modem Ring	<b>[Disabled]</b> [Enabled]	Determines the action taken when the system power is off and a modem connected to the serial port is ringing.
Auto Wake on S5	<b>[Disabled]</b> [Enabled]	Auto wake on S5, By Day of Month or Fixed time of every day.

S5 Long Run Test	<b>[Disabled]</b> [Enabled]	Enable : force to enable RTC S5 wake up, even if OS disables it. Support ipwrtest to do RTC S5 wakeup.
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## 2.5 Boot Menu

Boot Menu of InsydeH2O Setup Utility allows users to setting the boot options.

**Figure 2-5. Setup Utility Boot Menu**



**Table 2-5 Boot Menu setting**

BIOS Setting	Options	Description
Boot Type	[Dual Boot Type] [Legacy Boot Type] <b>[UEFI Boot Type]</b>	Select boot type to Dual type, Legacy type or UEFI type.
Quick Boot	[Disabled] <b>[Enabled]</b>	Allows InsydeH2O to skip certain tests while booting. This will decrease the time

		needed to boot the system.
Quiet Boot	[Disabled] <b>[Enabled]</b>	Disables or enables booting in Text Mode.
Network Stack	<b>[Disabled]</b> [Enabled]	Network Stack Support: Windows 8 BitLocker Unlock UEFI IPv4/IPv6 PXE Legacy PXE OPROM
PXE Boot capability	<b>[Disabled]</b> [Enabled]	Disabled : Support Network Stack UEFI PXE : IPv4/IPv6 Legacy : Legacy PXE OPROM only
Power Up In Standby Support	<b>[Disabled]</b> [Enabled]	Disable or enable Power Up In Standby Support. The PUIS feature set allows devices to be powered-up into the Standby power management state to minimize inrush current at power-up and to allow the host to sequence the spin-up of devices.
Storage PCI Option Rom access right Support	[Disabled] <b>[Enabled]</b>	Disable or enable storage PCI option rom access right. This feature will enable or disable storage PCI option rom being load and dispatched.
ESATA drive boot access right Support	[Disabled] <b>[Enabled]</b>	Disable or enable ESATA drive boot access right. This feature will allowed or deny boot up an

		ESATA storage device
Add Boot Options	[First][Last][ <b>Auto</b> ]	Position in Boot Order for Shell, Network and Removables.
ACPI Selection	[Acpi1.0B][Acpi3.0][Acpi4.0][ <b>Acpi5.0</b> ][Acpi6.0][Acpi6.1][Acpi6.2]	Select booting to Acpi3.0/Acpi1.0B.
USB Boot	[Disabled] [ <b>Enabled</b> ]	Disables or enables booting to USB boot devices.
EFI Device First	[Disabled] [ <b>Enabled</b> ]	Determine EFI device first or legacy device first. If enable, it is EFI device first. If disable, it is Legacy device first.
UEFI OS Fast Boot	[Disabled] [ <b>Enabled</b> ]	If enabled the system firmware does not initialize keyboard and check for firmware menu key.
USB Hot Key Support	[ <b>Disabled</b> ] [Enabled]	Enable/Disable to support USB hot key while booting. This will decrease the time needed to boot the system.
Timeout	<b>minimum = 0</b> <b>maximum = 10</b> <b>step = 1</b> <b>default = 0</b>	The number of seconds that the firmware will wait before booting the original default boot selection.
Automatic Failover	[Disabled] [ <b>Enabled</b> ]	Enable: if boot to default device fail, it will directly try to boot next device. Disable: if boot to default device fail, it will pop warning message then go into firmware UI.

EFI	EFI Internal Shell	EFI Boot Order Settings.
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## 2.6 Exit Menu

Exit Menu of InsydeH2O Setup Utility provide options for user to decide to save the changed setting or not.



**Table 2-6 Exit Menu setting**

BIOS Setting	Options	Description
Exit Saving Changes	No options	Exit system setup and save your changes.
Save Change Without Exit	No options	Save your changes and without exiting system.
Exit Discarding Changes	No options	Exit system setup and without saving your changes.
Load Optimal Defaults	No options	Load Optimal Defaults.

Load Custom Defaults	No options	Loads Custom Defaults.
Save Custom Defaults	No options	Save Custom Defaults
Discard Changes	No options	Discards Changes

## 2.7 General Help

User presses <F1> key in InsydeH2O Setup Utility to get the help text and hot key descriptions.

Figure 2-7.General Menu

